

GENEVA

CPU : MEROM
Chip Set : SANTAROSA CHIPSET
Remarks : Mobility Platform

Model Name : GENEVA
PBA Name : MAIN
PCB Code : BA41-XXXXX
Dev. Step : PV2
Revision : 1.0
T.R. Date :

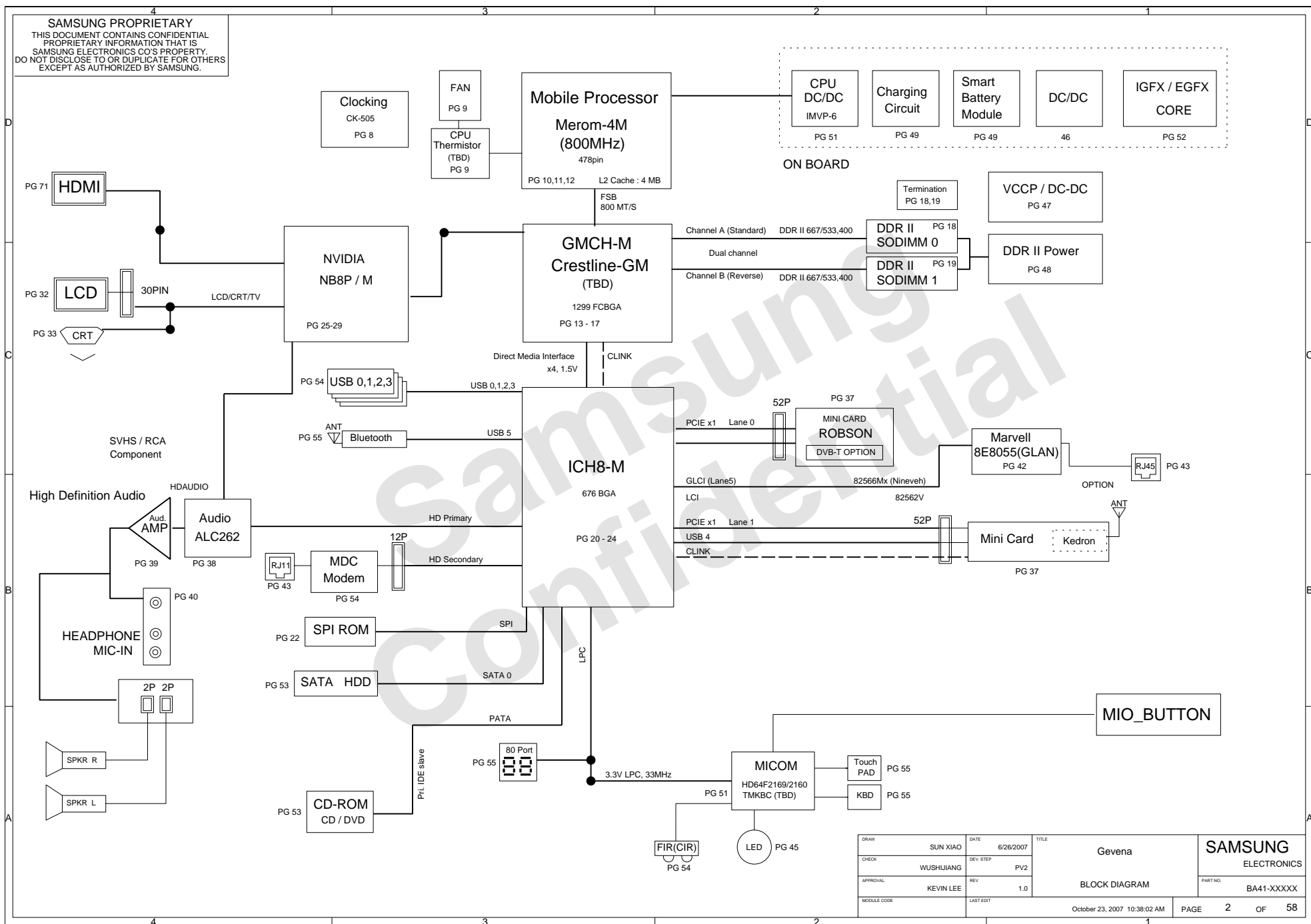
DRAW	CHECK	APPROVAL

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DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Geneva	SAMSUNG ELECTRONICS
CHECK	WUSHUIJANG	DEV. STEP	PV2	MILAN	PART NO.	
APPROVAL	KEVIN LEE	REV	1.0	COVER	BA41-XXXXX	
MODULE CODE		LAST EDIT	October 23, 2007 10:38:02 AM	PAGE	1	OF 58

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CHECK	WUSHUJIANG	DEV. STEP	PV2			
APPROVAL	KEVIN LEE	REV	1.0			
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BOARD INFORMATION

SCHEMATIC ANNOTATIONS AND BOARD INFORMATION

PCI Devices

Devices	IDSEL#	REQ/GNT#	Interrupts
Cardbus	AD25	3	B,C,D
DT PCI SLOT	AD22	1	B,C,D,C
MiniPCI SLOT	AD23	2	A,B
USB	AD29(internal)	-	USB2.0 #0 (USB0) : A USB2.0 #1 (USB1) : D USB2.0 #2 (USB4) : C USB2.0 #3 (USB5) : E USB2.0 #4 (EHCI) : H
Hub to PCI	AD30(internal)	-	-
LPC bridge/IDE/AC97/SMBUS	AD31(internal)	-	B
Internal MAC	AD24(internal)	-	E
AC Link	-	-	B
GLAN	-	-	F

Voltage Rails

VDC	Primary DC system power supply (7 to 21V)
VCC_CORE	Core Voltage for CPU
MCH_CORE	Core Voltage for CPU
ICH1_CORE	Core Voltage for CPU
P1.05V (VCCP)	VTT for CPU, Crestline & ICH8-M
P1.05V_M	1.05V switched power rail for ME (on in M0/M1)
P1.25V_M	1.25V switched power rail for ME (on in M0/M1)
P3.3V_M	3.3V switched power rail for ME (on in M0/M1)
P3.3V_A	3.3V always power rail (by KBC3_ALWS_ON)
MICOM_P3V	3.3V always power rail (for Micom)
LAN_3.3V	3.3V always power rail (for LAN)
P1.5V	1.5V switched off power rail (off in S3-S5)
P1.5V_AUX	1.5V switched on power rail
P2.5V	2.5V switched off power rail (off in S3-S5)
P1.8V	1.8V switched off power rail (off in S3-S5)
P1.8V_AUX	1.8V power rail for DDR
P0.9V	0.9V power rail for DDR
P3.3V	3.3V switched off power rail (off in S3-S5)
P3.3V_AUX	3.3V switched on power rail
PSV	5.0V switched off power rail (off in S3-S5)
PSV_AUX	5.0V switched on power rail

USB PORT Assign

PORT #	ASSIGNED TO
0	SYSTEM PORT 0
1	SYSTEM PORT 1
2	DMB
3	Expresas Card
4	DOCKING PORT 0
5	Bluetooth
6	Mini PCI Express
7	Aux Display
8	Test Port (RSVD)
9	WWAN/WIBRO (TBD)

PCI Express Assign

PORT #	ASSIGNED TO
0	PCI-E x1 Slot
1	Mini Card (Golan)
2	Mini Card (WIBRO : RSVD)
3	Expresas Card
4	DOCKING PORT 0
5	GLAN

Crystal / Oscillator

TYPE	FREQUENCY	DEVICE	USAGE
Crystal	32.768KHz	ICH8-M	Real Time Clock
Crystal	10MHz	MICOM	HD64F2169/2160
Crystal	14.318MHz	CLOCK-Generator	CK-505
Crystal	24.576MHz	Cardbus Controller	1394
Crystal	25MHz	LAN	Intel LAN
Crystal	27MHz (TBD)	VIDEO	PEG
Crystal	24.576MHz (TBD)	HD Audio	Audio

LCD Pannel Detect

(TBD)

Devices	Resolution	PANNEL_DETECT_0

I²C / SMB Address

Devices	Address	Hex	Bus
ICH8-m	Master	-	SMBUS Master
CPU Thermal Sensor	1001 110x	9Ch	Thermal Sensor
SODIMM0	1010 000x	A0h	-
SODIMM1	1010 010x	A4h	-
Thermal Sensor on SODIMM0	0011 000x	30h	-
Thermal Sensor on SODIMM1	0011 010x	34h	-
CK-505M (Clock Generator)	1101 001x	D2h	Clock, Unused Clock Output Disable
DB400 (PCI Express Clocks)	1101 110x	DCh	Clock Buffer for PCI Express
TBD	0100 1100	4Ch	Thermal Sensor
TBD : (LVDS BackLight Inverter)	0101 1000	58h	-
TBD : (ALS)	0111 0010	72h	Ambient Light Sensor
TBD : (AUX DISPLAY)	0011 110x	3Ch	EMA
LAN	1100 1000	C8h	82566
PCI Express Docking	TBD	TBD	TBD
TPM	TBD	TBD	TBD

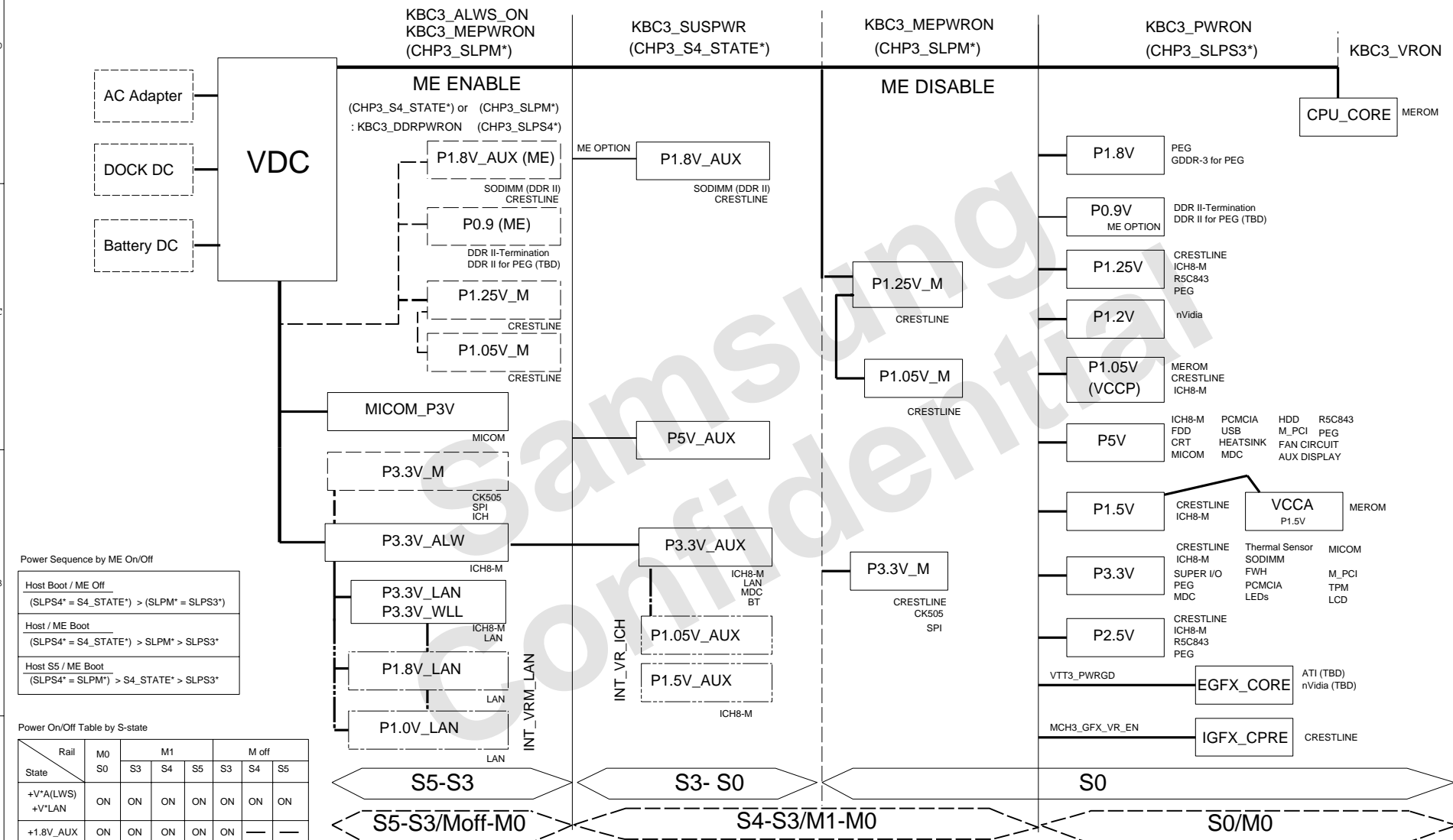
REVISION HISTORY

See rev notes for more information.

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APPROVAL	KEVIN LEE	REV	1.0	BOARD INFO		PART NO. BA41-XXXXX
MODULE CODE		LAST EDIT	October 23, 2007 10:38:02 AM	PAGE	3	OF 58

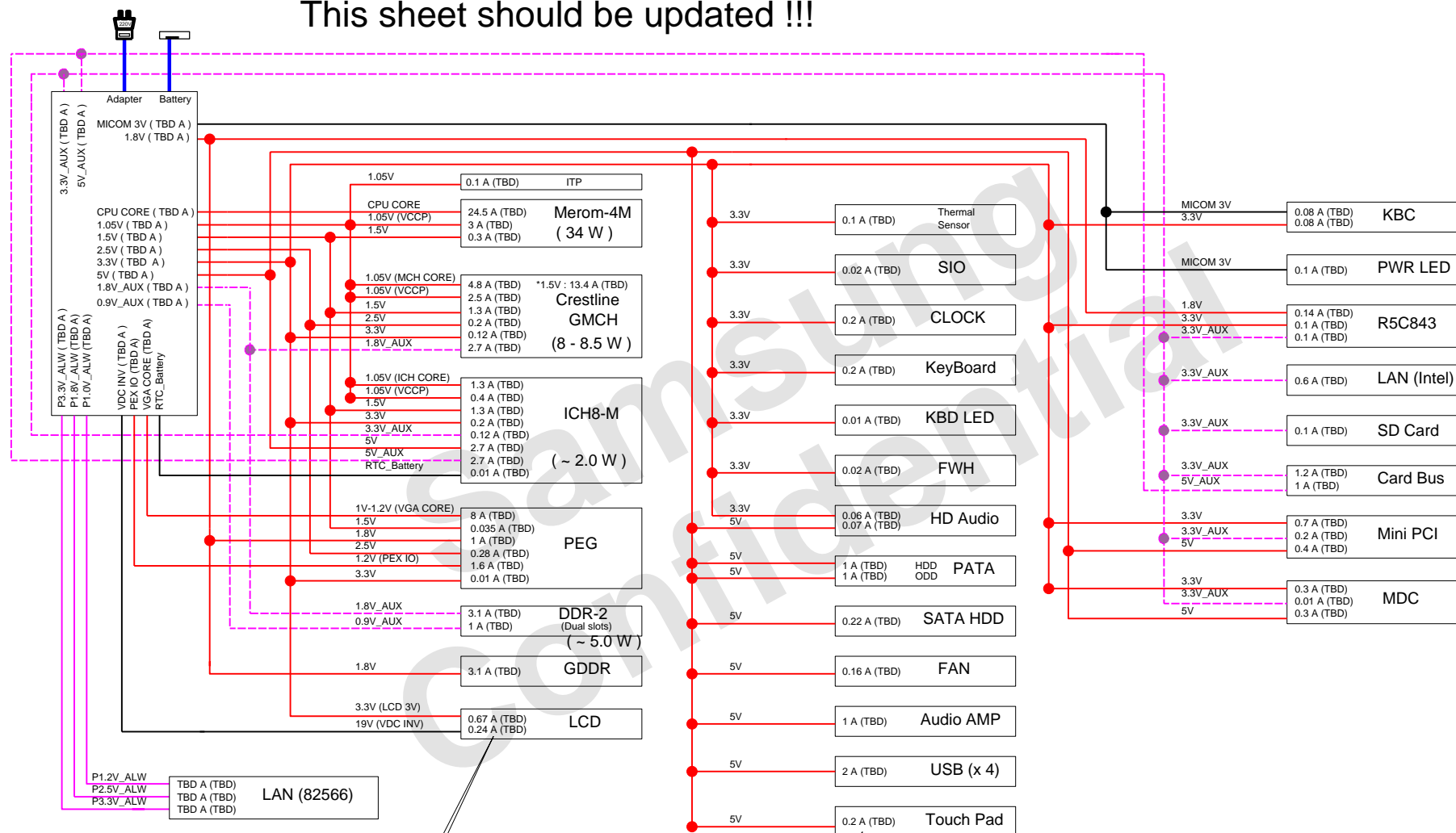
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POWER DIAGRAM



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APPROVAL	KEVIN LEE	REV	1.0	POWER DIAGRAM	PART NO.	BA41-XXXXX
MODULE CODE		LAST EDIT	October 23, 2007 10:38:02 AM	PAGE	4	OF 58

This sheet should be updated !!!



Value by Datasheet/Application notes (Value by measurement)

DRAW		DATE		TITLE		SAMSUNG ELECTRONICS	
SUN XIAO		6/26/2007		Gevena POWER RAILS			
CHECK		REV: STEP					
WUSHUJIANG		PV2					
APPROVAL		REV		POWER RAILS		PART NO.	
KEVIN LEE		1.0				BA41-XXXXX	
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	Battery	Adapter	

Host S5 / ME Boot
(SLPS4* = SLPM*) > S4_STATE* > SLPS3*

1) VCC_RTC

Rev. 0.5

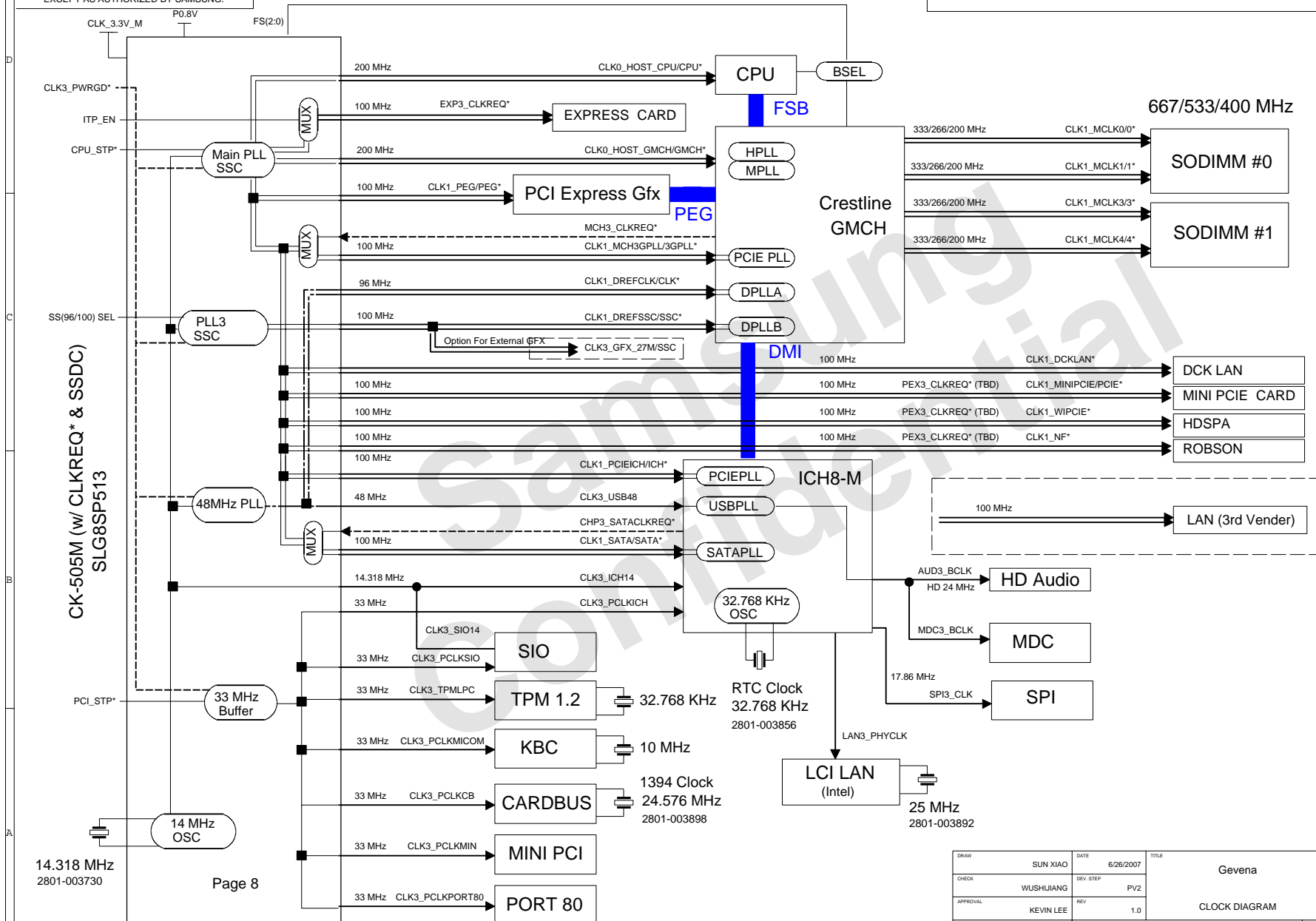


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CLOCK DISTRIBUTION

Rev. 0.8



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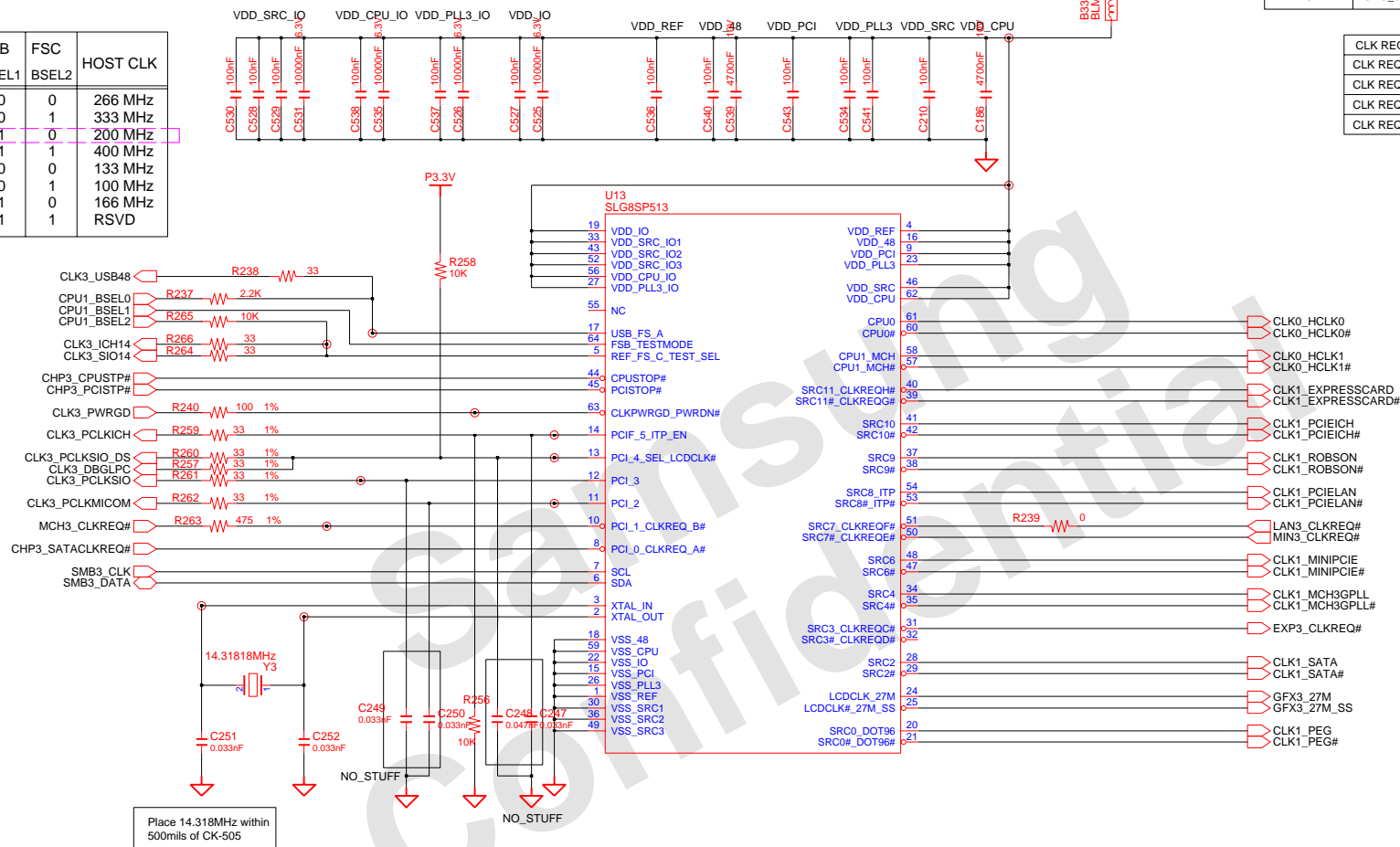
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FSA BSEL0	FSB BSEL1	FSC BSEL2	HOST CLK
0	0	0	266 MHz
0	0	1	333 MHz
0	1	0	200 MHz
0	1	1	400 MHz
1	0	0	133 MHz
1	0	1	100 MHz
1	1	0	166 MHz
1	1	1	RSVD

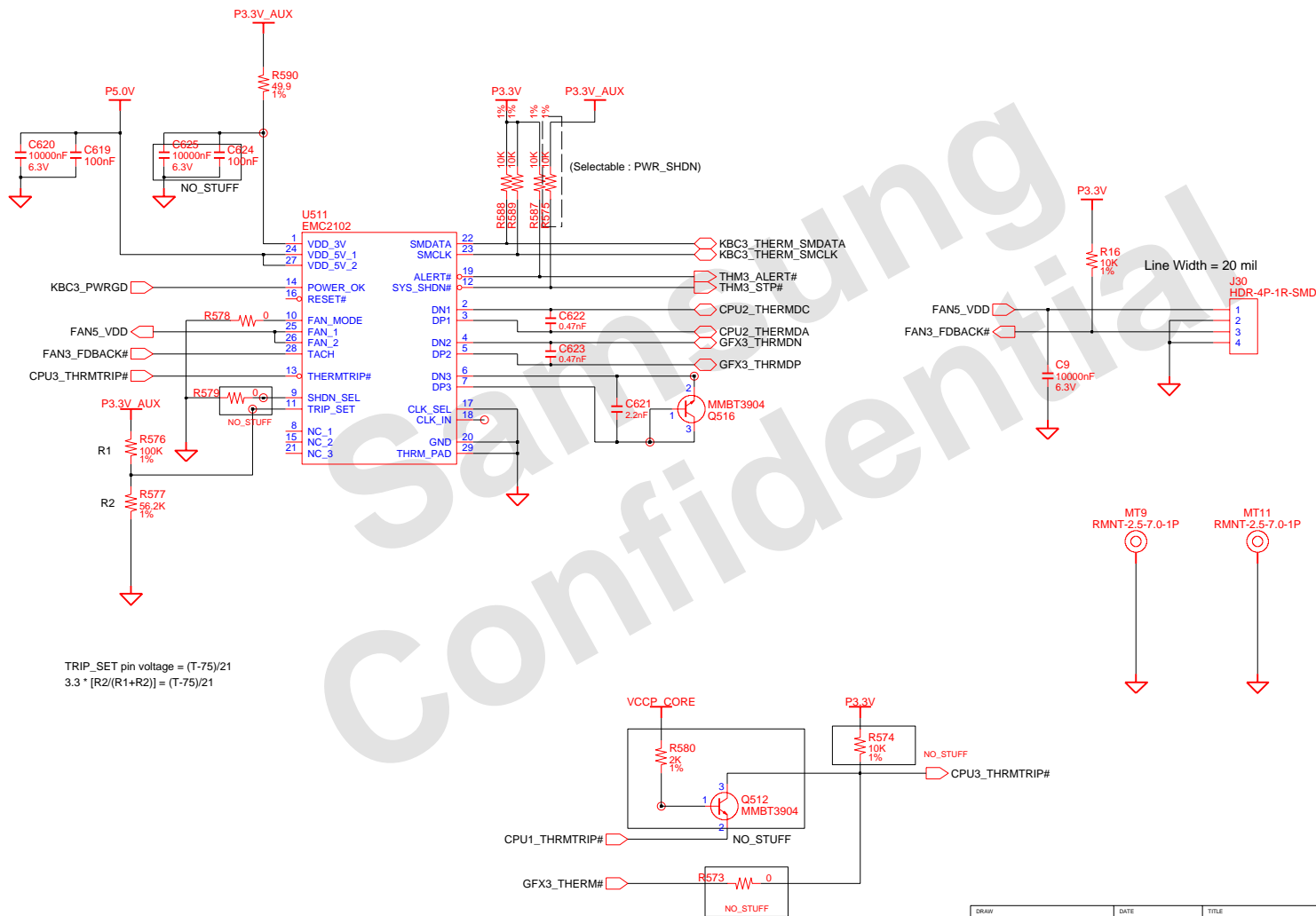
SEL_LCDCLK*	Pin 20/21	Pin 24/25
LOW	DOT_96/DOT_96#	LCDCLK/LCDCLK#
HIGH	SRC_0/SRC_0#	27M & 27M_SS

CLK REQ	DEVICE	SRC POR
CLK REQ A	SATA	SRC2
CLK REQ B	GMCH	SRC4
CLK REQ E	MINI CARD	SRC6
CLK REQ F	EXPRESS CARD	SRC8



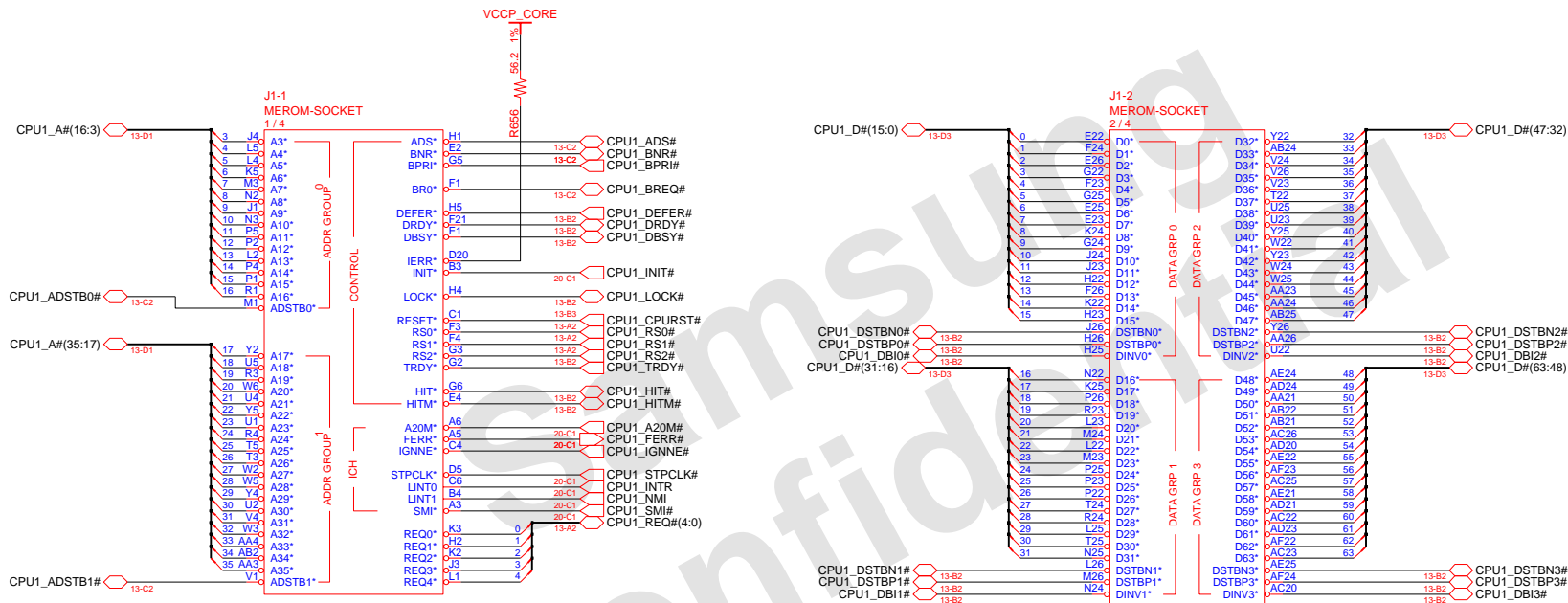
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APPROVAL	KEVIN LEE	REV	1.0					
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THERMAL SENSOR & FAN CONTROL

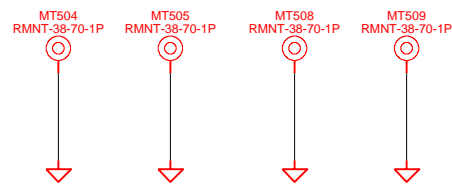


DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena THERMAL BLOCK THERMAL & FAN CONTROL	SAMSUNG ELECTRONICS
CHECK	WUSHUJIANG	DEV. STEP	PV2			PART NO. BA41-XXXXX
APPROVAL	KEVIN LEE	REV	1.0			
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CPU CONNECTOR PART NUMBER 3704-001153



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APPROVAL	KEVIN LEE	REV	1.0			
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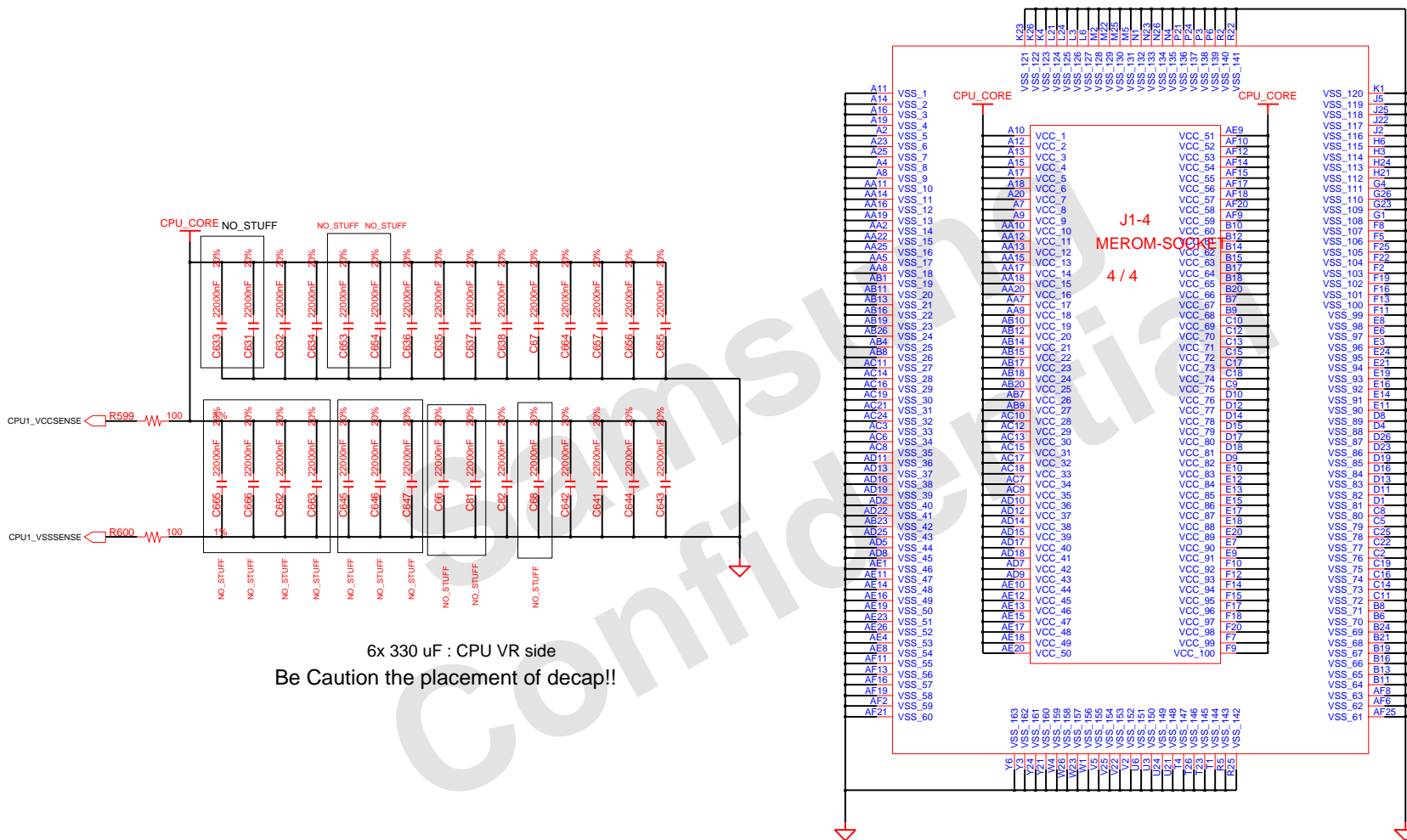
IMVP-6

*Yonah Processor (2.33 GHz / 800 MHz : TBD)

GND test points within 100mil of the VCC/VSSsense at the end of the line.
Route the VCC/VSSsense as a $Z_0=55\text{ohm}$ traces with equal length.
Observe 3:1 spacing b/w VCC/VSSsense lines and 25mil away
(preferred 50mil) from any other signal. And GND via 100mil away
from each of the VCC/VSS test point vias.

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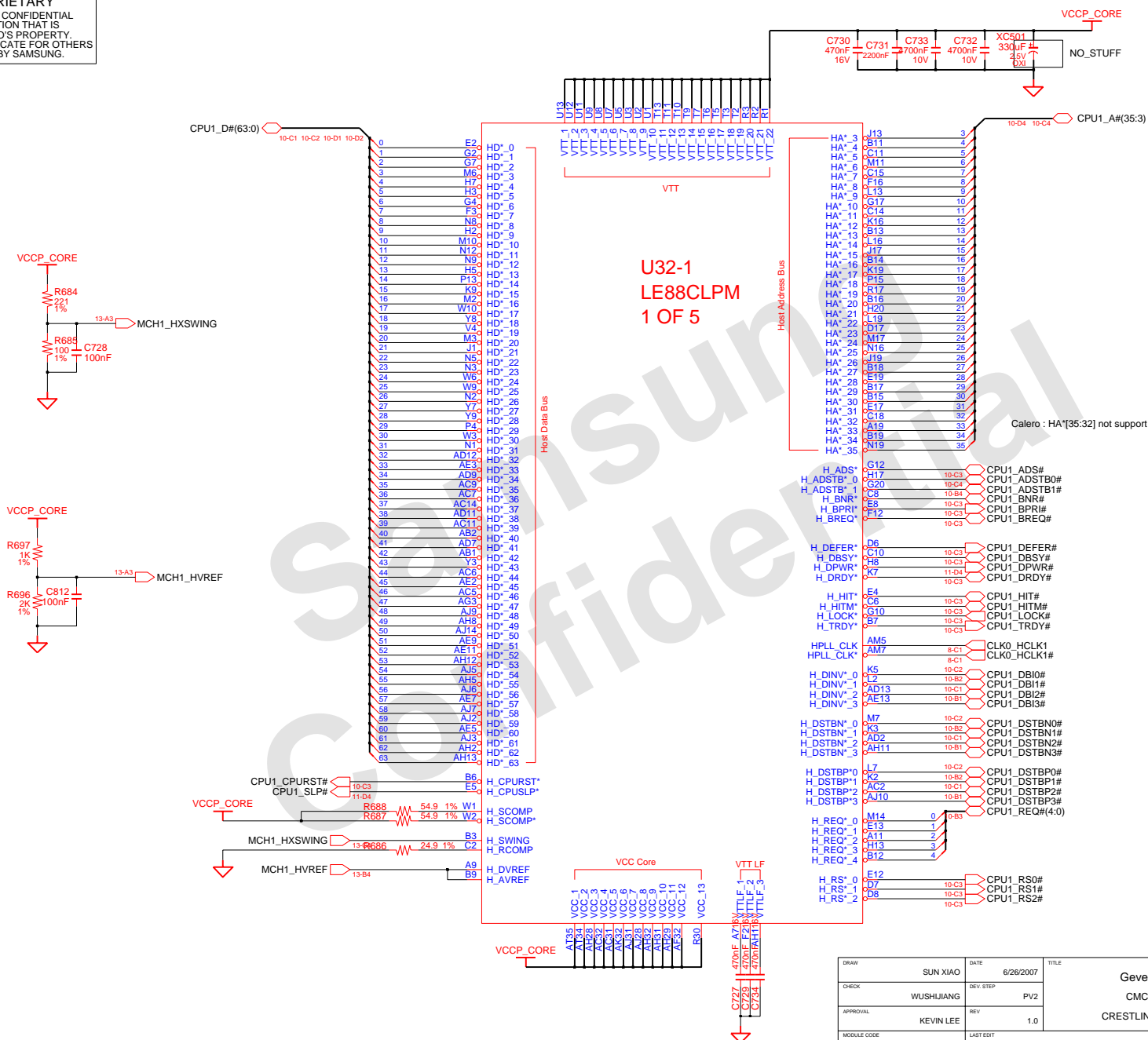
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CHECK	WUSHUJIANG	DEV. STEP	PV2		CPU
APPROVAL	KEVIN LEE	REV	1.0		MEROM(3/3)
MODULE CODE		LAST EDIT	October 23, 2007 10:38:02 AM	PAGE	12 OF 58

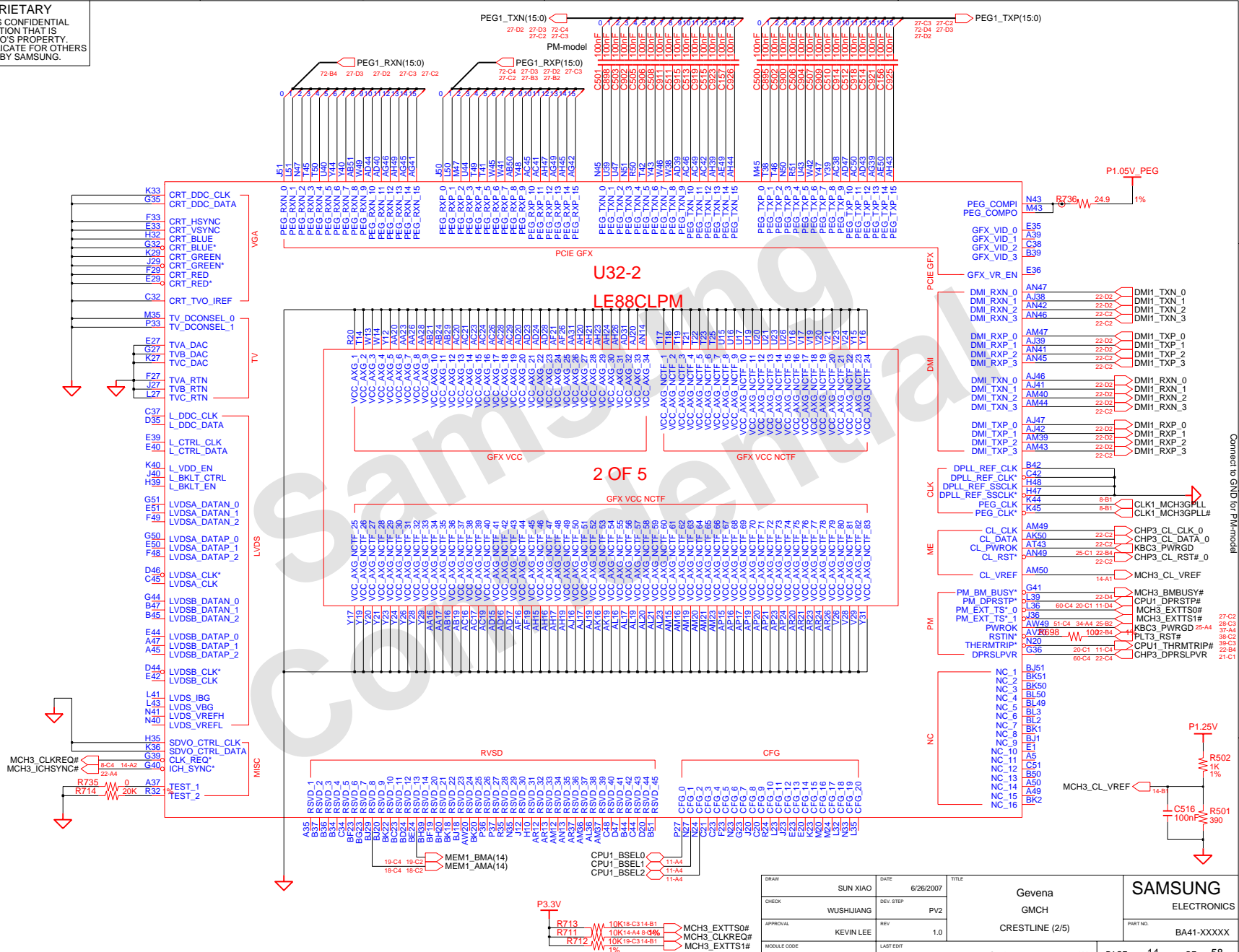
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BA41-XXXXX

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SUN XIAO		6/26/2007					
CHECK		REV. STEP		<div style="text-align: center;"> Gevena CMCH CRESTLINE (1/5) </div>		PART NO.	
WUSHUJIANG		PV2				BA41-XXXXX	
APPROVAL		REV					
KEVIN LEE		1.0		CRESTLINE (1/5)			
MODULE CODE		LAST EDIT		October 23, 2007 10:38:02 AM		PAGE 13 OF 58	

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MEM1_ADQ(63:0) 18-D4

MEM1_ABS0 18-B2 18-C4 BB19 SA_BS_0
MEM1_ABS1 18-B2 18-C4 BF29 SA_BS_1
MEM1_ABS2 18-B2 18-C4 BF29 SA_BS_2
MEM1_ADM(7:0) 18-B2 18-C4

MEM1_ADQS(7:0) 18-A4

MEM1_ADQS(7:0) 18-B4

MEM1_AMA(13:0) 18-C4 18-B4

MEM1_ACAS# 18-B2 18-B4 BL17 SA_CAS*
MEM1_ARAS# 18-B2 18-B4 BA19 SA_RAS*
MEM1_AWE# 18-B2 18-B4 AY20 SA_WE*
SA_RCVEN* 18-B2 18-B4

MEM1_CS0# 18-C2 18-C4 BK16 SM_CS*_0
MEM1_CS1# 18-C2 18-C4 BK16 SM_CS*_1
MEM1_CS2# 18-C2 18-C4 BE13 SM_CS*_2
MEM1_CS3# 18-C2 18-C4 BE13 SM_CS*_3

MEM1_ODT0 18-B2 18-B4 BJ15 SM_ODT_0
MEM1_ODT1 18-B2 18-B4 BJ14 SM_ODT_1
MEM1_ODT2 18-B2 18-B4 BJ14 SM_ODT_2
MEM1_ODT3 18-B2 18-B4 BE16 SM_ODT_3

SM_RCAMP_VOH BK31
SM_RCAMP_VOL BL31

Route as short as possible

SYSTEM MEMORY A

SYSTEM MEMORY B

DDR MUX

U32-3
LE88CLPM
3 OF 5

MEM1_VREF 19-C3 18-C3 57-C4
MEM1_VREF 19-C3 18-C3 57-C4

CLK1_MCLK0# 18-C4
CLK1_MCLK1# 18-C4
CLK1_MCLK3# 18-C4
CLK1_MCLK4# 19-B4

CLK1_MCLK0 18-C4
CLK1_MCLK1 18-C4
CLK1_MCLK3 18-C4
CLK1_MCLK4 19-C4

MEM1_CKE0 18-C2 18-B4
MEM1_CKE1 18-B4 18-B2
MEM1_CKE3 19-C2 19-B4
MEM1_CKE4 19-B4 19-B2

MEM1_BBS0 19-C4 19-B2
MEM1_BBS1 19-C4 19-B2
MEM1_BBS2 19-C4 19-B4
MEM1_BDM(7:0) 19-C4 19-B4

MEM1_BDQS(7:0) 19-A4
MEM1_BDQS(7:0) 19-B4
MEM1_BMA(13:0) 19-C4 19-D2

MEM1_BCAS# 19-B4 19-B2
MEM1_BRAS# 19-B4 19-B2
MEM1_BWE# 19-B4 19-B2

MEM1_BQ(63:0) 18-D4

DRAW: SUN XIAO, DATE: 6/26/2007, TITLE: Gevena, GMCH, CRESTLINE (3/5)
CHECK: WUSHUJIANG, DEV STEP: PV2
APPROVAL: KEVIN LEE, REV: 1.0
MODULE CODE: LAST EXT: October 23, 2007 10:38:02 AM, PAGE: 15 OF 58

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CFG#	Current Setting	(def.: default Option)
CFG(5)	DMIX2	DMIX4 (def.)
CFG(6)	Reserved	DDR-II (def.)
CFG(7)	DTT/Transportable	Mobile CPU (def.)
CFG(9)	PEG Reversal	Normal
CFG(16)	Dynamic ODT Disabled	Dynamic ODT Enabled (def.)
CFG(18)	VCC 1.05V (def.)	VCC 1.5V
CFG(19)	DMI Lane Normal	DMI Lane Reversal
CFG(20)	SDVO or PCIE X1 Only(def.)	SDVO and PCIE X1 Simultaneously

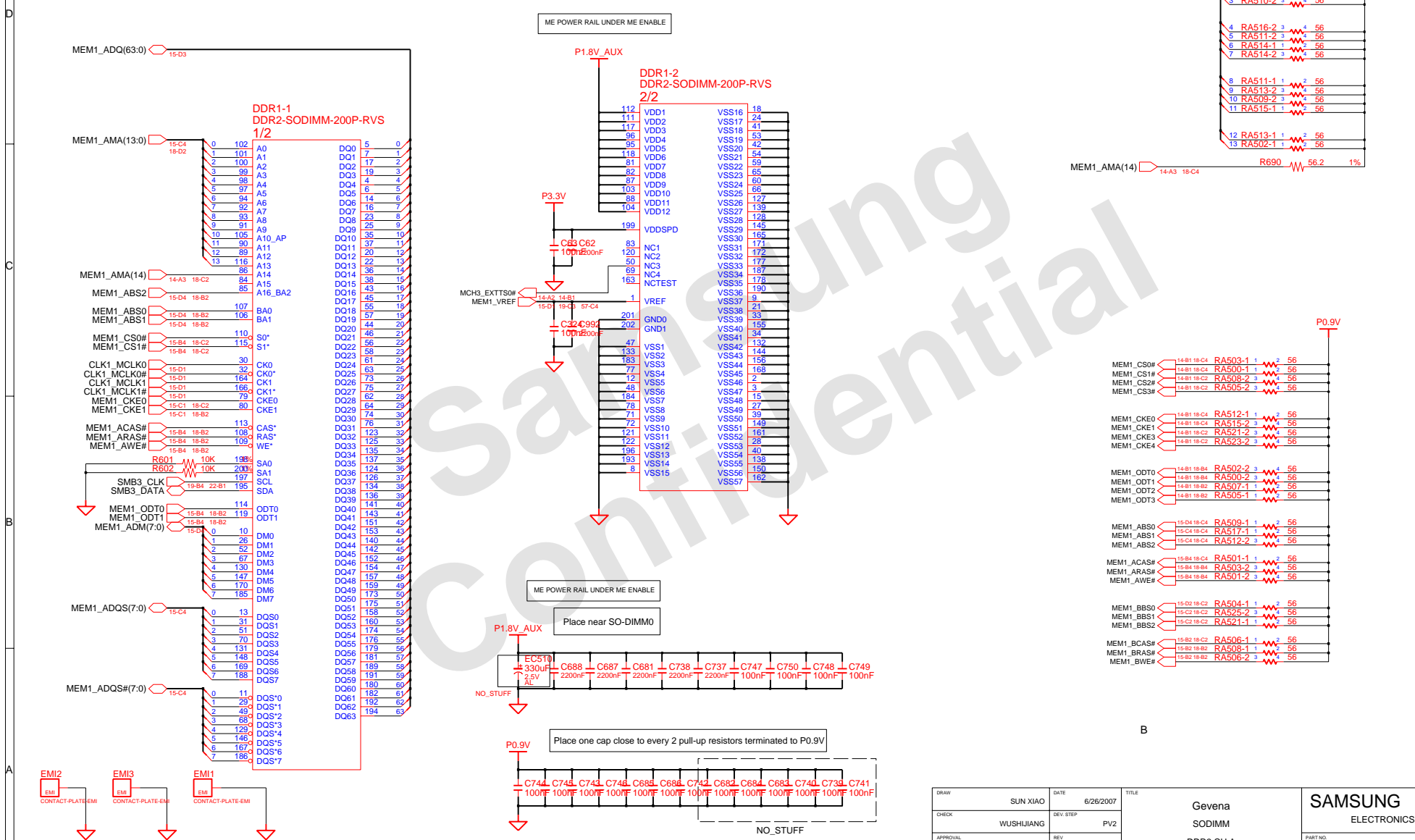
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CHECK	WUSHUJIANG	DEV STEP	PV2	Gevena	
APPROVAL	KEVIN LEE	REV	1.0	GMCH	
MODULE CODE		LAST EDIT		CRESTLINE (5/5)	

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*POCAFEb-11 Only (Remove in MP Model)		
Current Setting (def.: default Option)		
CFG#	Low	High
CFG(5)	DmIx2	DmIX4 (def.)
CFG(6)	Reserved	DDR-L (def.)
CFG(7)	DT/Transportable	Mobile CPU (def.)
CFG(9)	PEG Reversal	Normal
CFG(16)	Dynamic ODT Disabled	Dynamic ODT Enabled (def.)
CFG(18)	VCC 1.05V (def.)	VCC 1.5V
CFG(19)	DmI Lane Normal	DmI Lane Revers.
CFG(20)	SDVO or PCIE X1 (def.)	SDVO and PCIE X1 Simultaneously

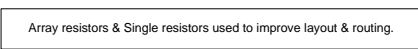
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Array resistors & Single resistors used to improve layout & routing.



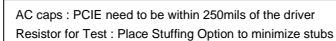
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APPROVAL	KEVIN LEE	REV	1.0					
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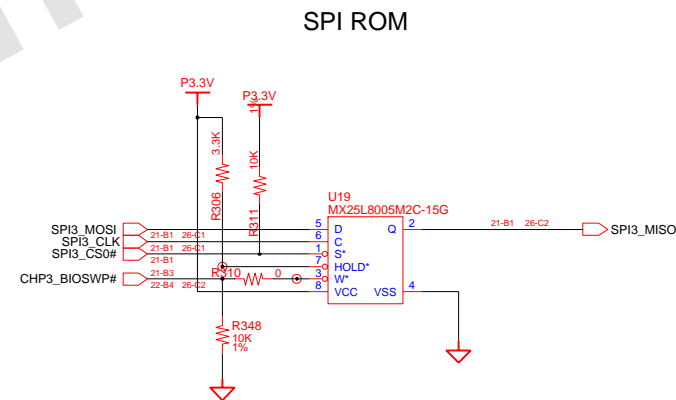
DDR SO-DIMM #1



COM-22C-015(1996.6.5) REV. 3

COM-22C-015(1996.6.5) REV. 3

D:/tingting/geneva/Geneva_pr_1023

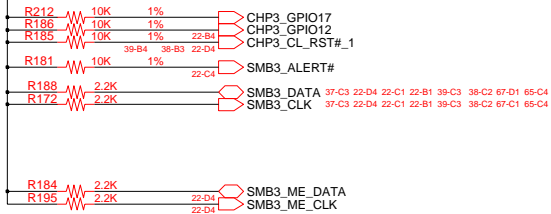


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SUN XIAO		6/26/2007		<div style="text-align: center;"> Gevena ICH8-M ICH8-M (3/5) </div>			
CHECK		DEV. STEP					
WUSHUJIANG		PV2				PART NO.	
APPROVAL		REV		1.0		BA41-XXXXX	
KEVIN LEE							
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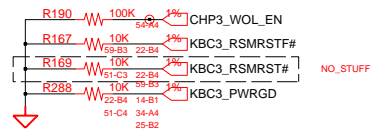
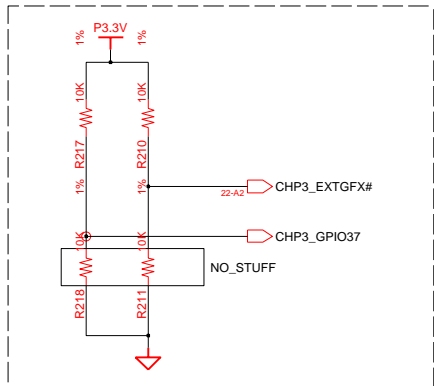
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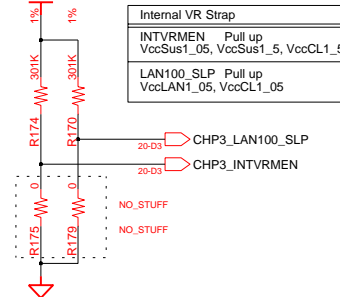
P3.3V_AUX



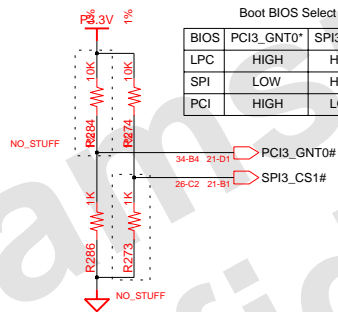
Model Dipendent



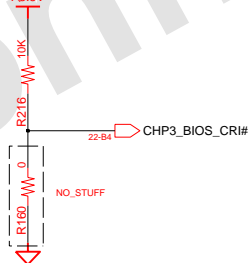
PRTC_BAT



Boot BIOS Select		
BIOS	PCI3_GNT0*	SPI3_CS1*
LPC	HIGH	HIGH
SPI	LOW	HIGH
PCI	HIGH	LOW



P3.3V



BIOS CRISIS RECOVER STRAP
PLACE NEAR KEYBOARD

DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena	SAMSUNG ELECTRONICS
CHECK	WUSHUJIANG	DEV. STEP	PV2		ICH8-M	
APPROVAL	KEVIN LEE	REV	1.0		ICH8-M STAP	PART NO. BA41-XXXXX
MODULE CODE				LAST EDIT	October 23, 2007 10:38:02 AM	PAGE 24 OF 58

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U36-1
NB8P-SE-H-N-A1/H
1 / 5

COMPONENTS:

REF	VALUE	TYPE	DESCRIPTION
1	C726	100nF	AH5
2	C727	100nF	AH6
3	C808	100nF	AG17
4	C809	100nF	AG18
5	C810	100nF	AG19
6	C811	100nF	AG20
7	C812	100nF	AG21
8	C813	100nF	AG22
9	C814	100nF	AG23
10	C815	100nF	AG24
11	C816	100nF	AG25
12	C817	100nF	AG26
13	C818	100nF	AG27
14	C819	100nF	AG28
15	C820	100nF	AG29
16	C821	100nF	AG30
17	C822	100nF	AG31
18	C823	100nF	AG32
19	C824	100nF	AG33
20	C825	100nF	AG34
21	C826	100nF	AG35
22	C827	100nF	AG36
23	C828	100nF	AG37
24	C829	100nF	AG38
25	C830	100nF	AG39
26	C831	100nF	AG40
27	C832	100nF	AG41
28	C833	100nF	AG42
29	C834	100nF	AG43
30	C835	100nF	AG44
31	C836	100nF	AG45
32	C837	100nF	AG46
33	C838	100nF	AG47
34	C839	100nF	AG48
35	C840	100nF	AG49
36	C841	100nF	AG50
37	C842	100nF	AG51
38	C843	100nF	AG52
39	C844	100nF	AG53
40	C845	100nF	AG54
41	C846	100nF	AG55
42	C847	100nF	AG56
43	C848	100nF	AG57
44	C849	100nF	AG58
45	C850	100nF	AG59
46	C851	100nF	AG60
47	C852	100nF	AG61
48	C853	100nF	AG62
49	C854	100nF	AG63
50	C855	100nF	AG64
51	C856	100nF	AG65
52	C857	100nF	AG66
53	C858	100nF	AG67
54	C859	100nF	AG68
55	C860	100nF	AG69
56	C861	100nF	AG70
57	C862	100nF	AG71
58	C863	100nF	AG72
59	C864	100nF	AG73
60	C865	100nF	AG74
61	C866	100nF	AG75
62	C867	100nF	AG76
63	C868	100nF	AG77
64	C869	100nF	AG78
65	C870	100nF	AG79
66	C871	100nF	AG80
67	C872	100nF	AG81
68	C873	100nF	AG82
69	C874	100nF	AG83
70	C875	100nF	AG84
71	C876	100nF	AG85
72	C877	100nF	AG86
73	C878	100nF	AG87
74	C879	100nF	AG88
75	C880	100nF	AG89
76	C881	100nF	AG90
77	C882	100nF	AG91
78	C883	100nF	AG92
79	C884	100nF	AG93
80	C885	100nF	AG94
81	C886	100nF	AG95
82	C887	100nF	AG96
83	C888	100nF	AG97
84	C889	100nF	AG98
85	C890	100nF	AG99
86	C891	100nF	AG100
87	C892	100nF	AG101
88	C893	100nF	AG102
89</			

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U36-4
NB8P-SE-H-N-A1/H
4 / 5

Pin	Description	ACTIVATE
GPIO(0)	HDMI DETECT	HIGH
GPIO(1)	TV DETECT	NC
GPIO(2)	PWM BRIGHTNESS CONTROL	HIGH
GPIO(3)	LCD VDD On ENABLE	HIGH
GPIO(4)	LCD Backlight On/OFF	HIGH
GPIO(5)	GPU Voltage ID0	HIGH=1.0V, LOW=1.1V
GPIO(6)	GPU Voltage ID1	NC
GPIO(7)	GPU Voltage ID2	NC
GPIO(8)	Thermal diode Alert	LOW
GPIO(9)	Fan Control	NC
GPIO(10)	TBD	NC
GPIO(11)	HDTV enable	HIGH
GPIO(12)	HDTV DET	NC

Pin List:

Pin 1-16: FBVDD_1, FBVDD_2, FBVDD_3, FBVDD_4, FBVDD_6, FBVDD_7, FBVDD_8, FBVDD_9, FBVDD_10, FBVDD_11, FBVDD_12, FBVDD_13, FBVDD_14, FBVDD_15, FBVDD_17, FBVDD_18, FBVDD_19, FBVDD_20, FBVDD_1, FBVDD_2, FBVDD_3, FBVDD_4, FBVDD_6, FBVDD_7, FBVDD_8, FBVDD_9, FBVDD_10, FBVDD_11, FBVDD_12, FBVDD_13, FBVDD_14, FBVDD_15, FBVDD_17, FBVDD_18, FBVDD_19, FBVDD_20.

Pin 17-32: FBVTT_1, FBVTT_2, FBVTT_3, FBVTT_4, FBVTT_5, FBVTT_6, FBVTT_7, FBVTT_8, FBVTT_9, FBVTT_10, FBVTT_11, FBVTT_12, FBVTT_13, FBVTT_14, FBVTT_15, FBVTT_16, FBVTT_17, FBVTT_18, FBVTT_1, FBVTT_2, FBVTT_3, FBVTT_4, FBVTT_5, FBVTT_6, FBVTT_7, FBVTT_8, FBVTT_9, FBVTT_10, FBVTT_11, FBVTT_12, FBVTT_13, FBVTT_14, FBVTT_15, FBVTT_16, FBVTT_17, FBVTT_18.

Pin 33-48: FBVDD_1, FBVDD_2, FBVDD_3, FBVDD_4, FBVDD_6, FBVDD_7, FBVDD_8, FBVDD_9, FBVDD_10, FBVDD_11, FBVDD_12, FBVDD_13, FBVDD_14, FBVDD_15, FBVDD_17, FBVDD_18, FBVDD_19, FBVDD_20, FBVDD_1, FBVDD_2, FBVDD_3, FBVDD_4, FBVDD_6, FBVDD_7, FBVDD_8, FBVDD_9, FBVDD_10, FBVDD_11, FBVDD_12, FBVDD_13, FBVDD_14, FBVDD_15, FBVDD_17, FBVDD_18, FBVDD_19, FBVDD_20.

Pin 49-64: FBVTT_1, FBVTT_2, FBVTT_3, FBVTT_4, FBVTT_5, FBVTT_6, FBVTT_7, FBVTT_8, FBVTT_9, FBVTT_10, FBVTT_11, FBVTT_12, FBVTT_13, FBVTT_14, FBVTT_15, FBVTT_16, FBVTT_17, FBVTT_18, FBVTT_1, FBVTT_2, FBVTT_3, FBVTT_4, FBVTT_5, FBVTT_6, FBVTT_7, FBVTT_8, FBVTT_9, FBVTT_10, FBVTT_11, FBVTT_12, FBVTT_13, FBVTT_14, FBVTT_15, FBVTT_16, FBVTT_17, FBVTT_18.

Pin 65-80: FBVDD_1, FBVDD_2, FBVDD_3, FBVDD_4, FBVDD_6, FBVDD_7, FBVDD_8, FBVDD_9, FBVDD_10, FBVDD_11, FBVDD_12, FBVDD_13, FBVDD_14, FBVDD_15, FBVDD_17, FBVDD_18, FBVDD_19, FBVDD_20, FBVDD_1, FBVDD_2, FBVDD_3, FBVDD_4, FBVDD_6, FBVDD_7, FBVDD_8, FBVDD_9, FBVDD_10, FBVDD_11, FBVDD_12, FBVDD_13, FBVDD_14, FBVDD_15, FBVDD_17, FBVDD_18, FBVDD_19, FBVDD_20.

Pin 81-96: FBVTT_1, FBVTT_2, FBVTT_3, FBVTT_4, FBVTT_5, FBVTT_6, FBVTT_7, FBVTT_8, FBVTT_9, FBVTT_10, FBVTT_11, FBVTT_12, FBVTT_13, FBVTT_14, FBVTT_15, FBVTT_16, FBVTT_17, FBVTT_18, FBVTT_1, FBVTT_2, FBVTT_3, FBVTT_4, FBVTT_5, FBVTT_6, FBVTT_7, FBVTT_8, FBVTT_9, FBVTT_10, FBVTT_11, FBVTT_12, FBVTT_13, FBVTT_14, FBVTT_15, FBVTT_16, FBVTT_17, FBVTT_18.

Pin 97-112: FBVDD_1, FBVDD_2, FBVDD_3, FBVDD_4, FBVDD_6, FBVDD_7, FBVDD_8, FBVDD_9, FBVDD_10, FBVDD_11, FBVDD_12, FBVDD_13, FBVDD_14, FBVDD_15, FBVDD_17, FBVDD_18, FBVDD_19, FBVDD_20, FBVDD_1, FBVDD_2, FBVDD_3, FBVDD_4, FBVDD_6, FBVDD_7, FBVDD_8, FBVDD_9, FBVDD_10, FBVDD_11, FBVDD_12, FBVDD_13, FBVDD_14, FBVDD_15, FBVDD_17, FBVDD_18, FBVDD_19, FBVDD_20.

Pin 113-128: FBVTT_1, FBVTT_2, FBVTT_3, FBVTT_4, FBVTT_5, FBVTT_6, FBVTT_7, FBVTT_8, FBVTT_9, FBVTT_10, FBVTT_11, FBVTT_12, FBVTT_13, FBVTT_14, FBVTT_15, FBVTT_16, FBVTT_17, FBVTT_18, FBVTT_1, FBVTT_2, FBVTT_3, FBVTT_4, FBVTT_5, FBVTT_6, FBVTT_7, FBVTT_8, FBVTT_9, FBVTT_10, FBVTT_11, FBVTT_12, FBVTT_13, FBVTT_14, FBVTT_15, FBVTT_16, FBVTT_17, FBVTT_18.

Pin 129-144: FBVDD_1, FBVDD_2, FBVDD_3, FBVDD_4, FBVDD_6, FBVDD_7, FBVDD_8, FBVDD_9, FBVDD_10, FBVDD_11, FBVDD_12, FBVDD_13, FBVDD_14, FBVDD_15, FBVDD_17, FBVDD_18, FBVDD_19, FBVDD_20, FBVDD_1, FBVDD_2, FBVDD_3, FBVDD_4, FBVDD_6, FBVDD_7, FBVDD_8, FBVDD_9, FBVDD_10, FBVDD_11, FBVDD_12, FBVDD_13, FBVDD_14, FBVDD_15, FBVDD_17, FBVDD_18, FBVDD_19, FBVDD_20.

Pin 145-160: FBVTT_1, FBVTT_2, FBVTT_3, FBVTT_4, FBVTT_5, FBVTT_6, FBVTT_7, FBVTT_8, FBVTT_9, FBVTT_10, FBVTT_11, FBVTT_12, FBVTT_13, FBVTT_14, FBVTT_15, FBVTT_16, FBVTT_17, FBVTT_18, FBVTT_1, FBVTT_2, FBVTT_3, FBVTT_4, FBVTT_5, FBVTT_6, FBVTT_7, FBVTT_8, FBVTT_9, FBVTT_10, FBVTT_11, FBVTT_12, FBVTT_13, FBVTT_14, FBVTT_15, FBVTT_16, FBVTT_17, FBVTT_18.

Pin 161-176: FBVDD_1, FBVDD_2, FBVDD_3, FBVDD_4, FBVDD_6, FBVDD_7, FBVDD_8, FBVDD_9, FBVDD_10, FBVDD_11, FBVDD_12, FBVDD_13, FBVDD_14, FBVDD_15, FBVDD_17, FBVDD_18, FBVDD_19, FBVDD_20, FBVDD_1, FBVDD_2, FBVDD_3, FBVDD_4, FBVDD_6, FBVDD_7, FBVDD_8, FBVDD_9, FBVDD_10, FBVDD_11, FBVDD_12, FBVDD_13, FBVDD_14, FBVDD_15, FBVDD_17, FBVDD_18, FBVDD_19, FBVDD_20.

Pin 177-192: FBVTT_1, FBVTT_2, FBVTT_3, FBVTT_4, FBVTT_5, FBVTT_6, FBVTT_7, FBVTT_8, FBVTT_9, FBVTT_10, FBVTT_11, FBVTT_12, FBVTT_13, FBVTT_14, FBVTT_15, FBVTT_16, FBVTT_17, FBVTT_18, FBVTT_1, FBVTT_2, FBVTT_3, FBVTT_4, FBVTT_5, FBVTT_6, FBVTT_7, FBVTT_8, FBVTT_9, FBVTT_10, FBVTT_11, FBVTT_12, FBVTT_13, FBVTT_14, FBVTT_15, FBVTT_16, FBVTT_17, FBVTT_18.

Pin 193-208: FBVDD_1, FBVDD_2, FBVDD_3, FBVDD_4, FBVDD_6, FBVDD_7, FBVDD_8, FBVDD_9, FBVDD_10, FBVDD_11, FBVDD_12, FBVDD_13, FBVDD_14, FBVDD_15, FBVDD_17, FBVDD_18, FBVDD_19, FBVDD_20, FBVDD_1, FBVDD_2, FBVDD_3, FBVDD_4, FBVDD_6, FBVDD_7, FBVDD_8, FBVDD_9, FBVDD_10, FBVDD_11, FBVDD_12, FBVDD_13, FBVDD_14, FBVDD_15, FBVDD_17, FBVDD_18, FBVDD_19, FBVDD_20.

Pin 209-224: FBVTT_1, FBVTT_2, FBVTT_3, FBVTT_4, FBVTT_5, FBVTT_6, FBVTT_7, FBVTT_8, FBVTT_9, FBVTT_10, FBVTT_11,

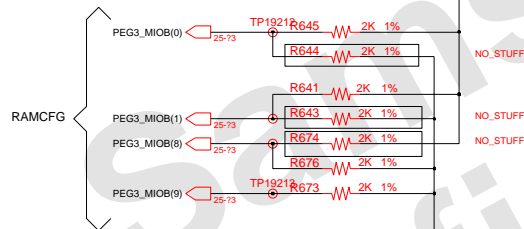
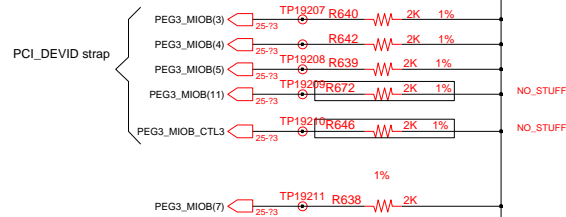
[illegible]

COM-22C-015(1996.6.5) REV. 3 D:\tingting\geneva\Geneva_pr_1023

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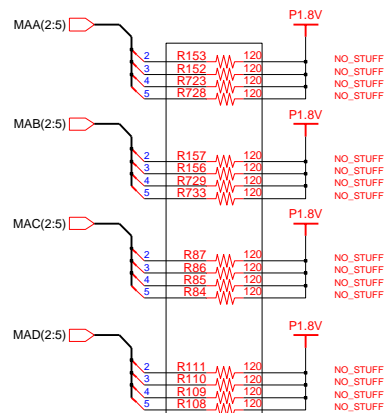
PCI_DEVID strap

	R646	R672	R640	R639	R642
NB8P-SE	NO_STUFF	NO_STUFF	STUFF	NO_STUFF	STUFF
NB8M-GS	0	0	1	1	1
	NO_STUFF	NO_STUFF	STUFF	STUFF	STUFF
	0	0	1	1	1



RAMCFG

	R674	R676	R641	R643
SS 256Mbit	STUFF	NO_STUFF	STUFF	NO_STUFF
IF 256Mbit	STUFF	NO_STUFF	NO_STUFF	STUFF
SS 512Mbit	NO_STUFF	STUFF	STUFF	NO_STUFF
IF 512Mbit	NO_STUFF	STUFF	NO_STUFF	STUFF



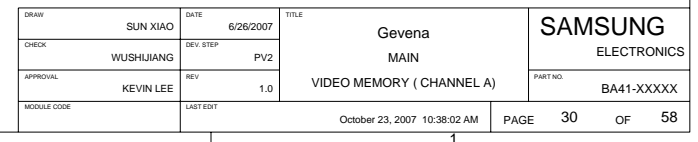
Straps	Pin # (Rev.A02)	Descriptions
SUB_VENDOR	MIOAD(1)	0 : No BIOS 1 : Read from BIOS
RAMCFG(3:0) [9,8,1,0]	MIOB(9) MIOB(8) MIOB(1) MIOB(0)	0111 : SAMSUNG GDDR3 256Mbit 0101 : INFINEON GDDR3 256Mbit 0011 : SAMSUNG GDDR3 512Mbit 0001 : INFINEON GDDR3 512Mbit
CRYSTAL(1:0)	MIOB(2) MIOB(6)	01 : 14.318 MHz 10 : 27 MHz 11 : Unknown 00 : 13.5 MHz
TV_MODE(1:0)	MIOAD(7) MIOAD(10)	00 : SECAM 01 : NTSC 10 : PAL 11 : CRT
PCI_DEVID(4:0) [CTL3,11,3,5,4]	MIOB_CTL(3) MIOB(11) MIOB(3) MIOB(5) MIOB(4)	NB8M-GS: 00111 NB8M-SE: 01000 NB8M-GT: 00110 NB8P-GS: 00111 NB8P-SE: 00101 NB8P-GT: 01000
ROM_TYPE(1:0)	MIOB(10) MIOBVSYN	NO ROM(NC)
USER STRAP	MIOAD(2:5)	EDID
GPIO(12:0)	Sheet 25	Refer to Sheet 25

Test Options for GPIO should be updated..

Samsung		Infineon	
256Mbit	512Mbit	256Mbit	512Mbit
K4J55323QG (1.2/1.4/1.6/2.0) K4J55323QF (1.4/1.6/2.0)	K4J52324QC (1.2/1.4/1.6/2.0)	HYB18H256321AFL20(2.0) HYB18H256321AFL16(1.6) HYB18H256324AF-20(2.0) HYB18H256321AF-14(1.4) HYB18H256321AF-12(1.2)	HYB18H512321AFL20(2.0) HYB18H512321AFL16(1.6) HYB18H512324AF-20(1.6) HYB18H512321AF-14(1.4) HYB18H512321AF-12(1.2)
8M*32BIT	16M*32BIT	8M*32BIT	16M*32BIT

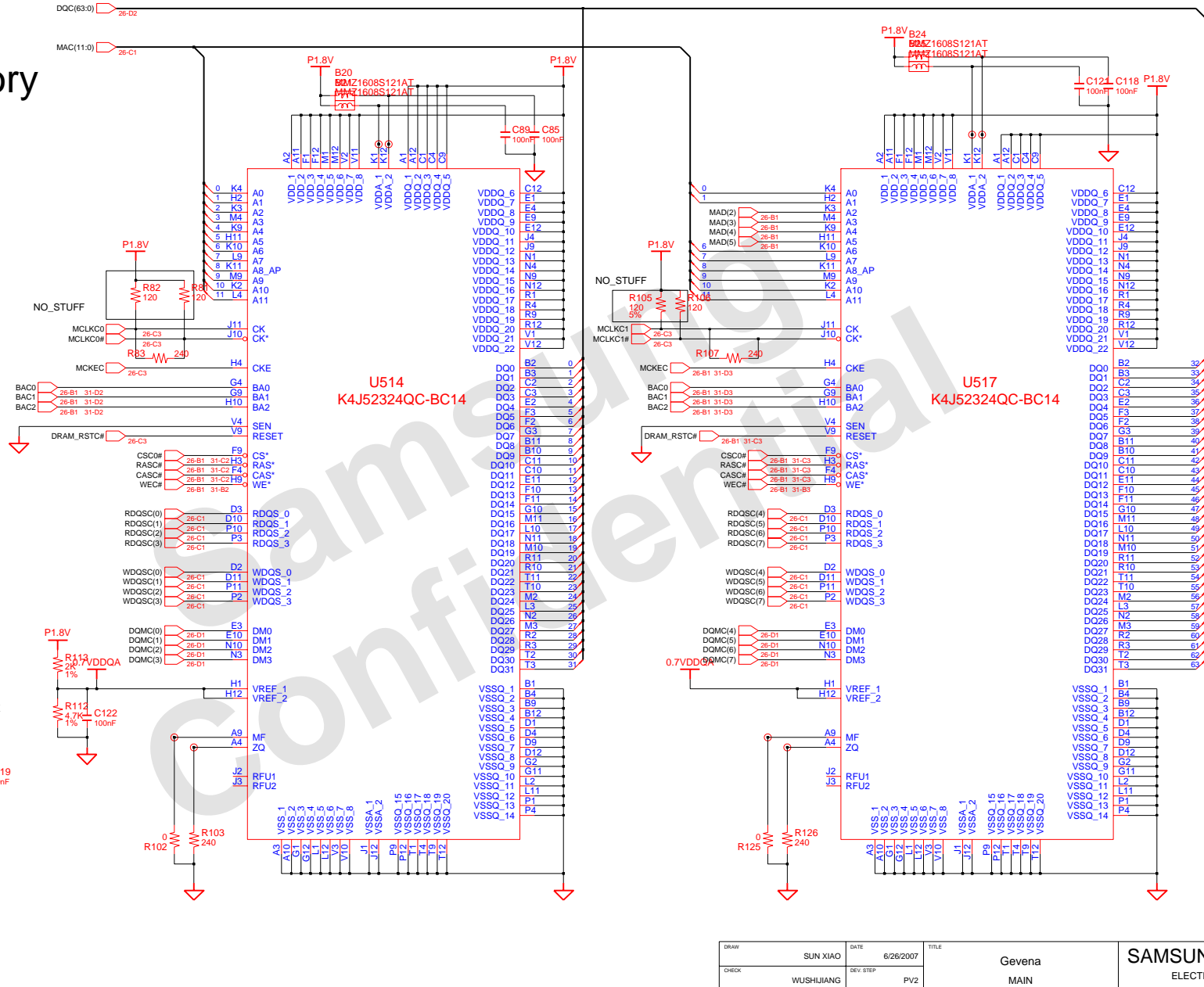
DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena	SAMSUNG ELECTRONICS PART NO. BA41-XXXXX
CHECK	WUSHUJIANG	DEV. STEP	PV2		NB8P	
APPROVAL	KEVIN LEE	REV	1.0		NB8P STRAP	
MODULE CODE		LAST EDIT		October 23, 2007 10:38:02 AM	PAGE	29 OF 58

Video Memory (A Channel)



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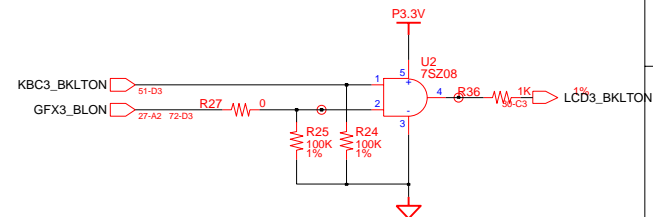
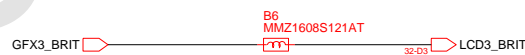
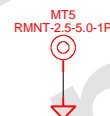
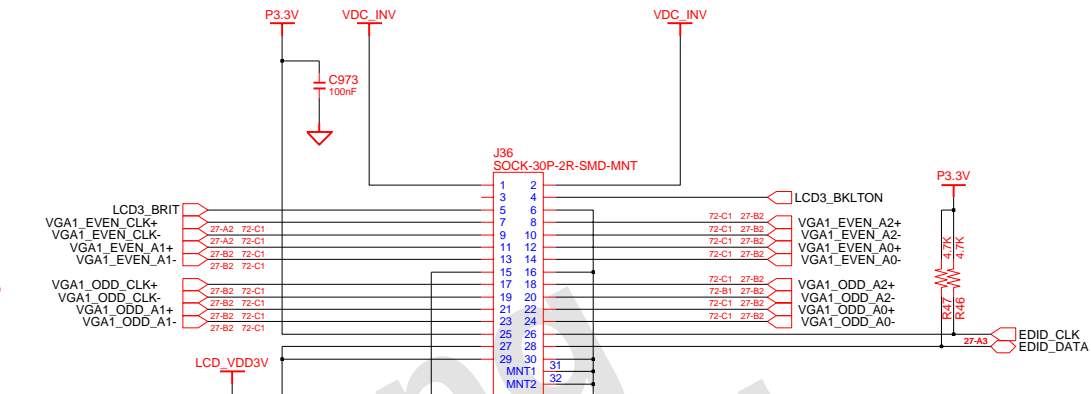
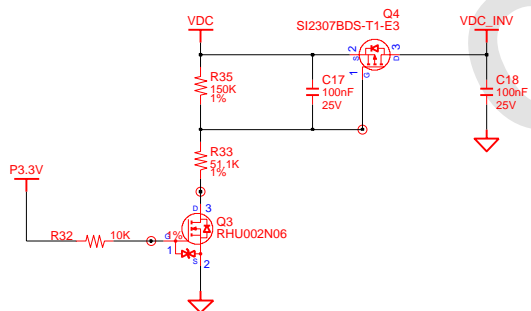
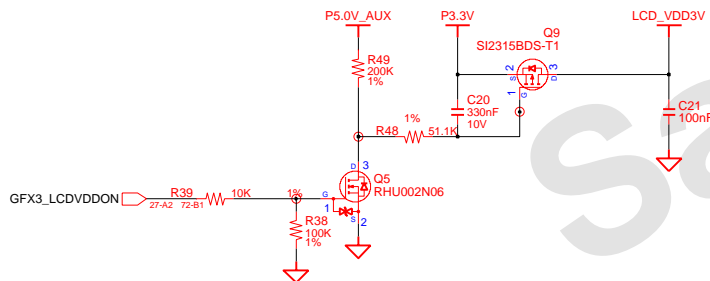
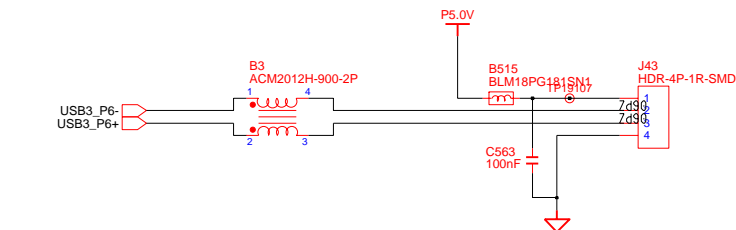
Video Memory (C Channel)



DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena
CHECK	WUSHUJIANG	DEV. STEP	PV2	MAIN	Gevena
APPROVAL	KEVIN LEE	REV	1.0	VIDEO MEMORY (CHANNEL B)	MAIN
MODULE CODE		LAST EDIT	October 23, 2007 10:38:02 AM	PAGE	31 OF 58

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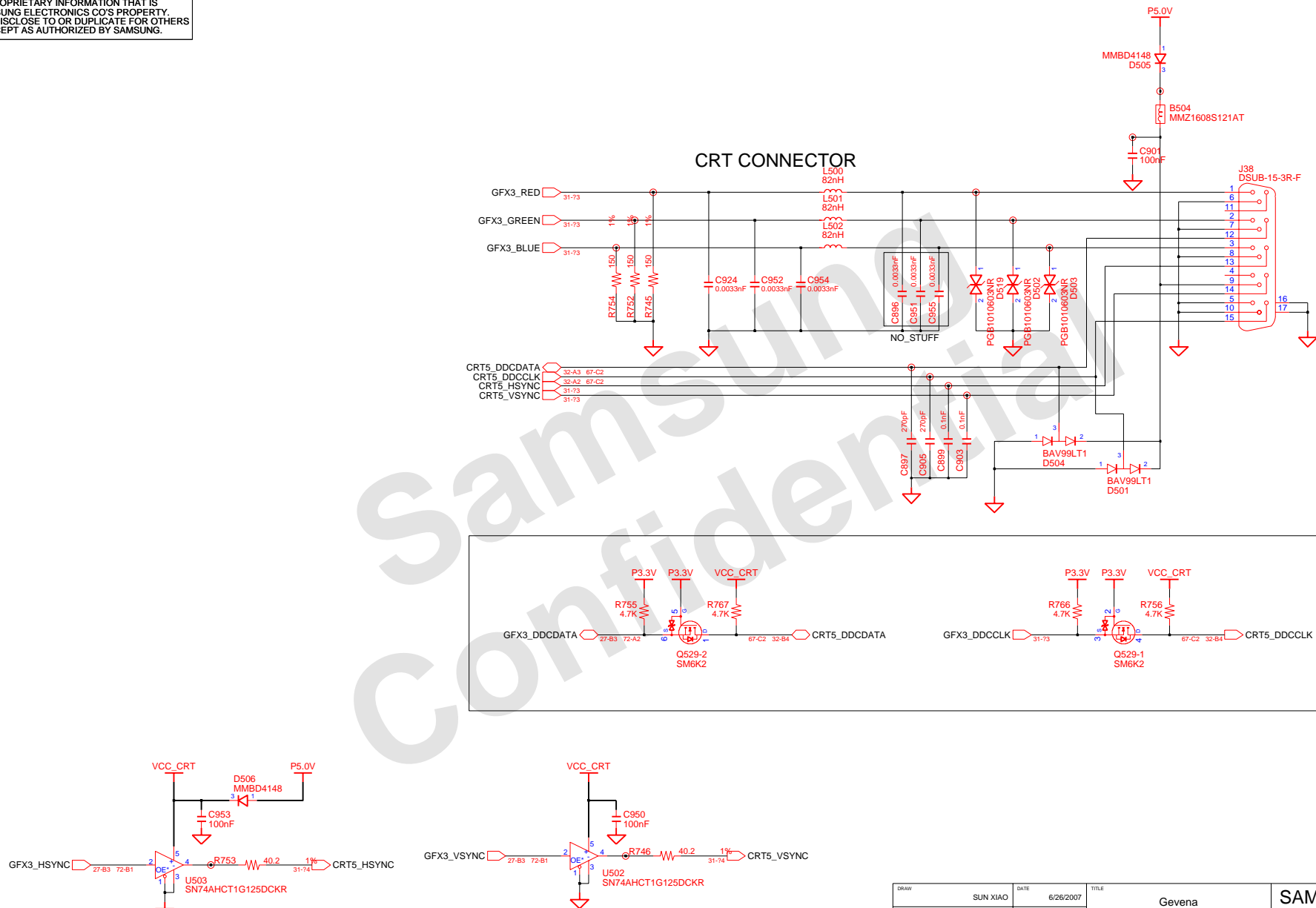
USB CAMERA FUNCTION



DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena	SAMSUNG
CHECK	WUSHUIJIANG	DEV. STEP	PV2	LCD CONNECTER & SPEED SPECTRUM	ELECTRONICS	
APPROVAL	KEVIN LEE	REV	1.0		PART NO.	BA41-XXXXX
MODULE CODE		LAST EDIT	October 23, 2007 10:38:02 AM	PAGE	32	OF 58

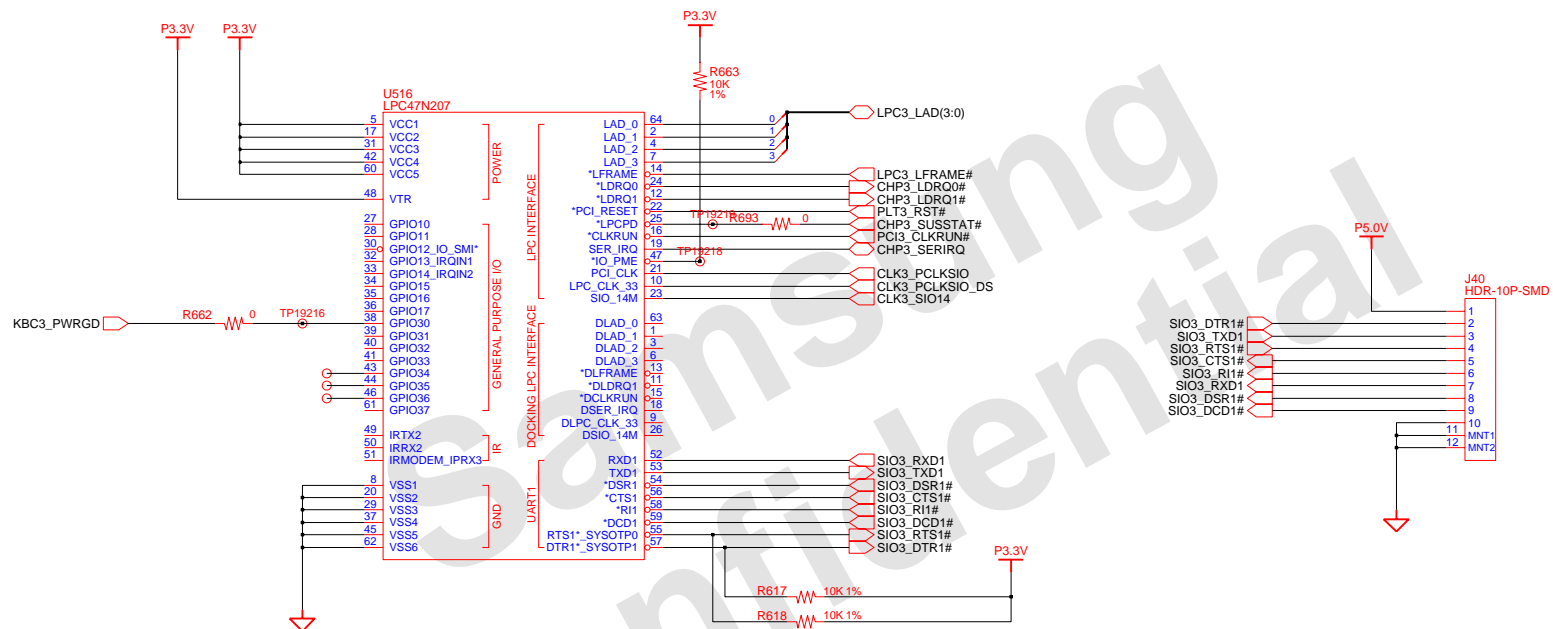
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CRT CONNECTOR



DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena
CHECK	WUSHUIJANG	DEV. STEP	PV2		MIAN
APPROVAL	KEVIN LEE	REV	1.0		CRT PORT
MODULE CODE		LAST EDIT		October 23, 2007 10:38:02 AM	
					PAGE 33 OF 58
					SAMSUNG ELECTRONICS
					PART NO. BA41-XXXXX

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Option

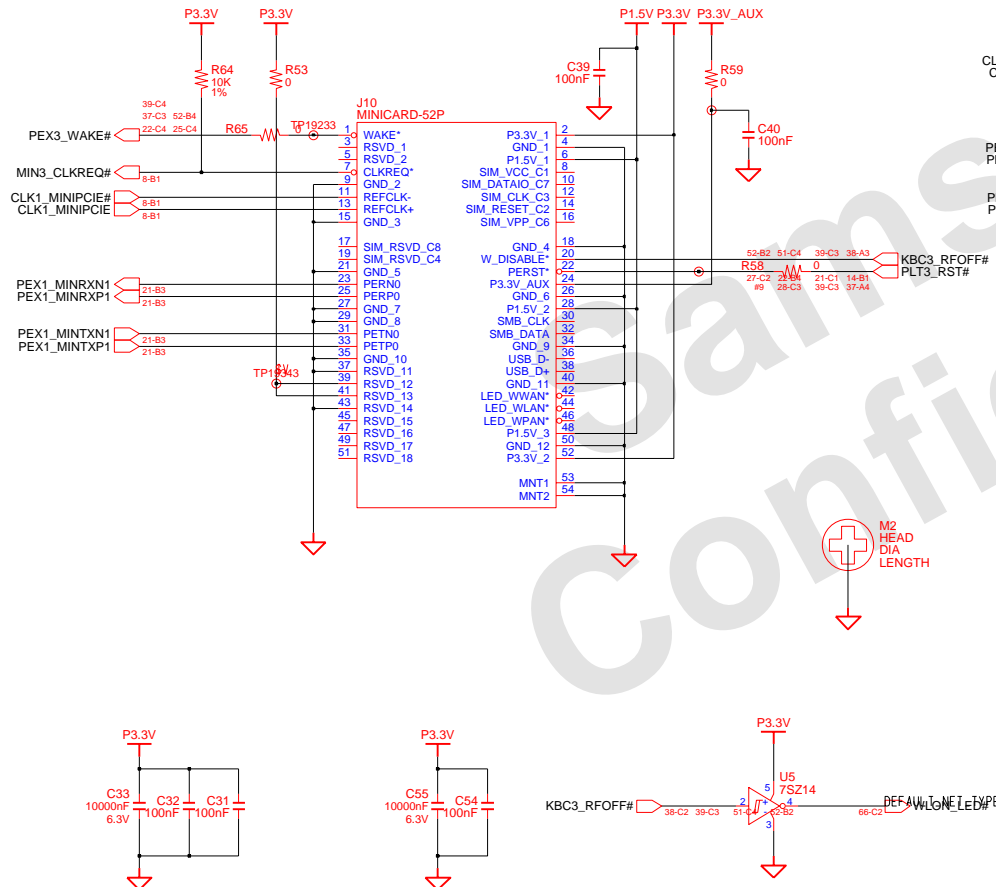
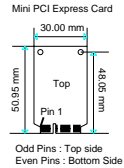
DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena	SAMSUNG
CHECK	WUSHUJIANG	DEV. STEP	PV2	SIO CHIPSET	ELECTRONICS	
APPROVAL	KEVIN LEE	REV	1.0		PART NO.	BA41-
MODULE CODE		LAST EDIT	October 23, 2007 10:38:02 AM	PAGE	34	OF 68

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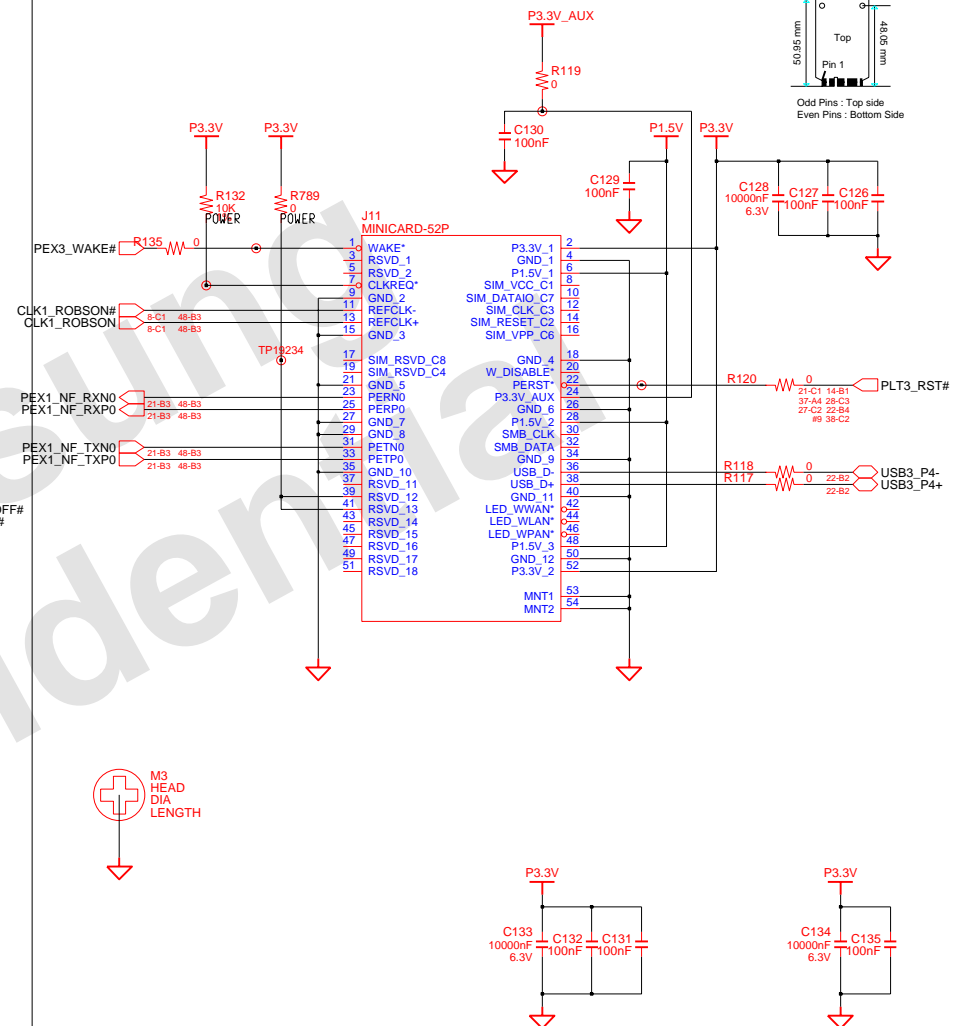
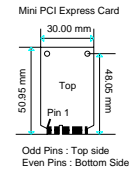
D:/tingting/geneva/Geneva_pr_102

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Mini Card



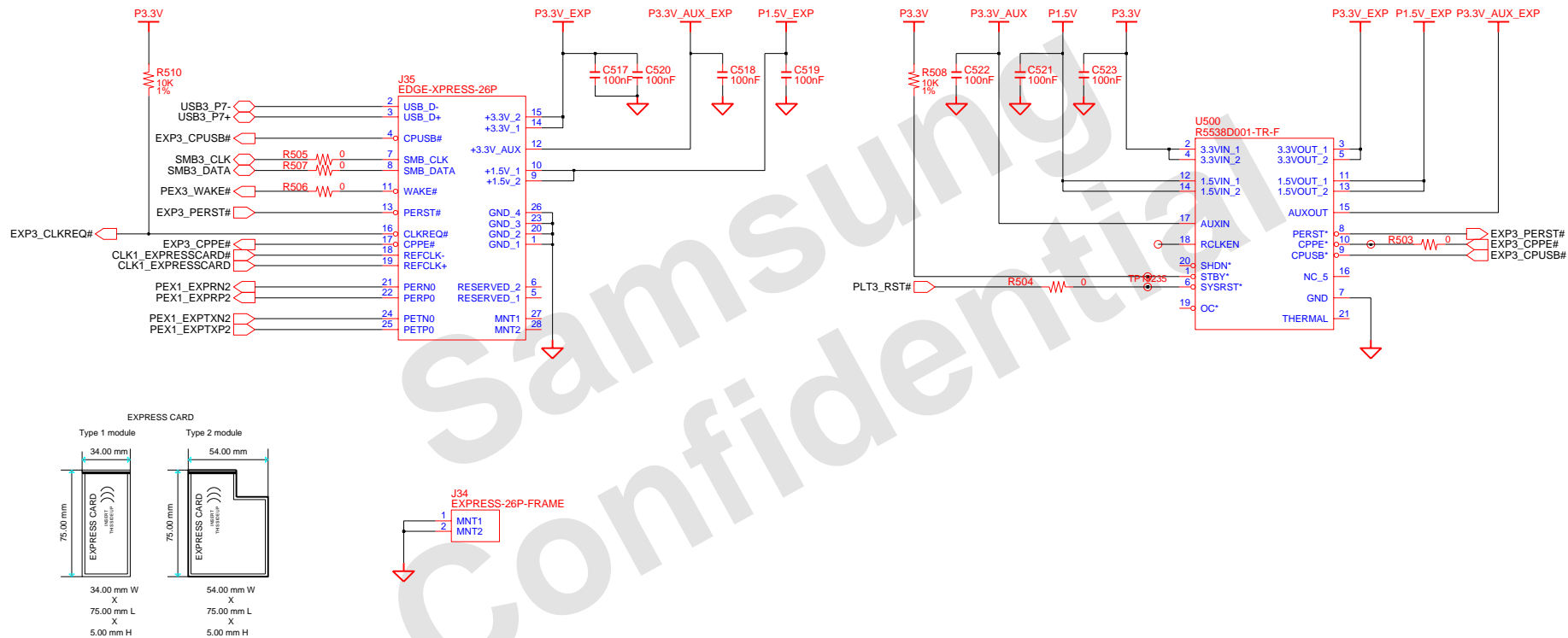
MINI CARD FOR ROBSON



DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena MINI CARD	SAMSUNG ELECTRONICS
CHECK	WUSHUJIANG	DEV. STEP	PV2			PART NO. BA41-XXXXX
APPROVAL	KEVIN LEE	REV	1.0		FRO BOBSON AND DVB-T	
MODULE CODE		LAST EDIT				
				October 23, 2007 10:38:02 AM	PAGE	36 OF 58

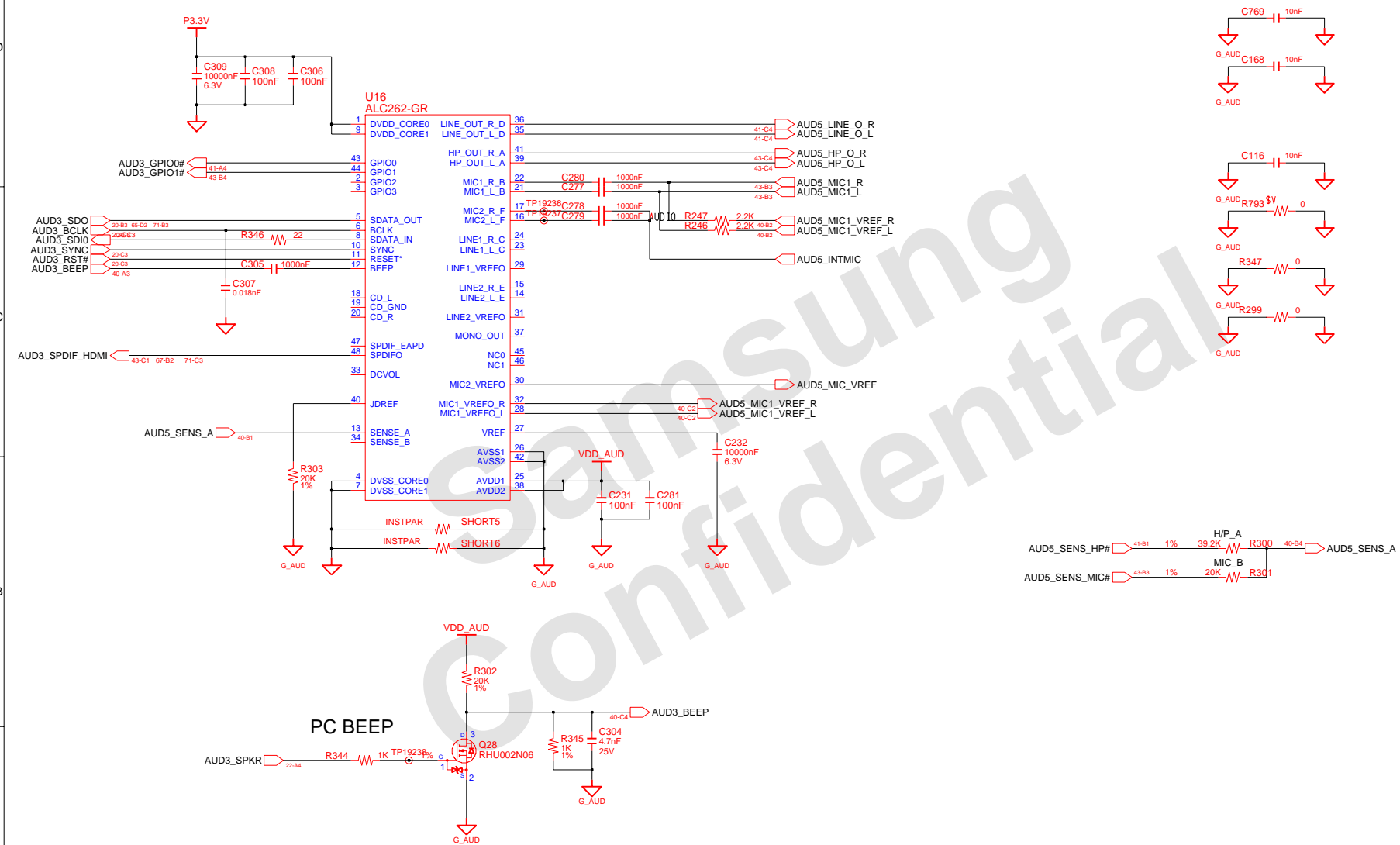
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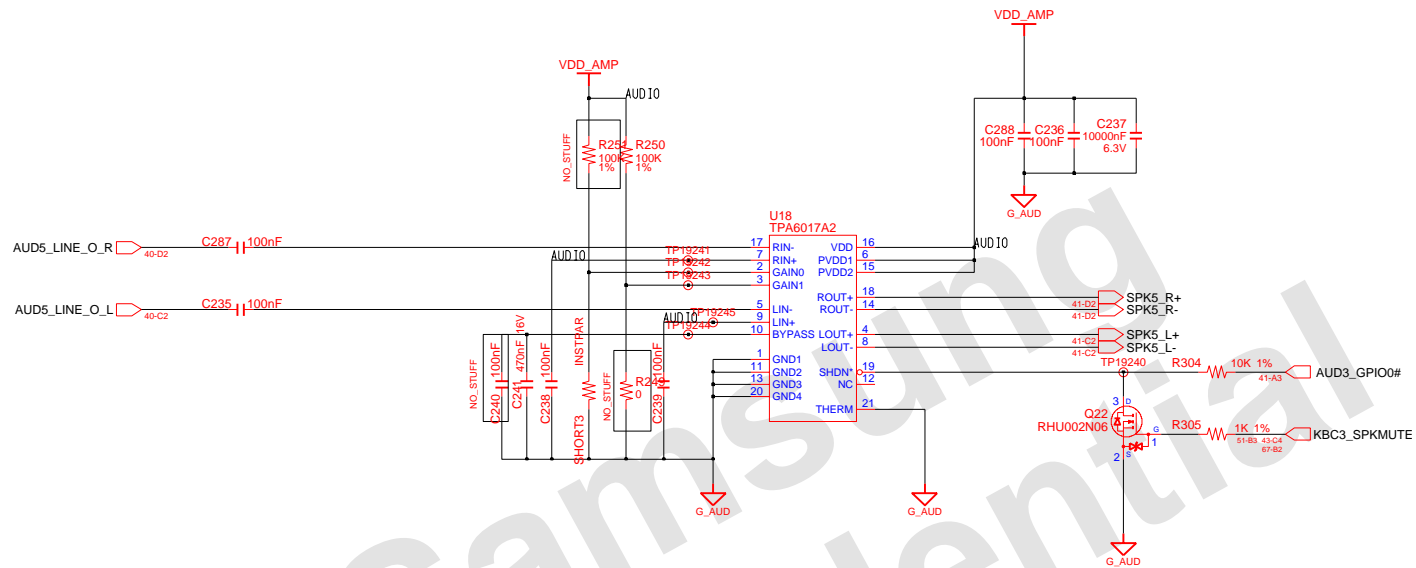
DRAW	SUN XIAO	DATE	6/27/2007	TITLE	Geneva MIO BOARD EXPRESS CARD	SAMSUNG ELECTRONICS PART NO. BA41-XXXX
CHECK	WUSHIJIANG	DEV. STEP	PV2			
APPROVAL	KEVIN LEE	REV	1.0			
MODULE CODE		LAST EDIT	October 23, 2007 10:38:02 AM	PAGE	37 OF 60	

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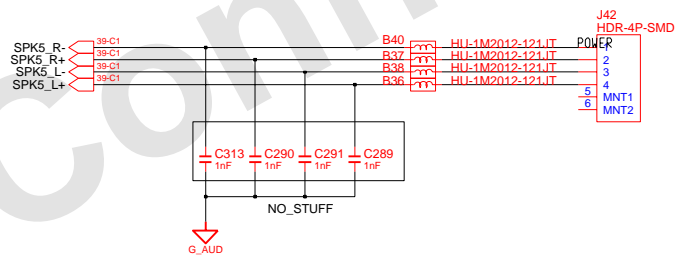


DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena	SAMSUNG
CHECK	WUSHUJIANG	DEV. STEP	PV2	AUDIO CODEC	ELECTRONICS	
APPROVAL	KEVIN LEE	REV	1.0	FRO HDMI	PART NO.	BA41-XXXXX
MODULE CODE		LAST EDIT	October 23, 2007 10:38:02 AM	PAGE	38	OF 58

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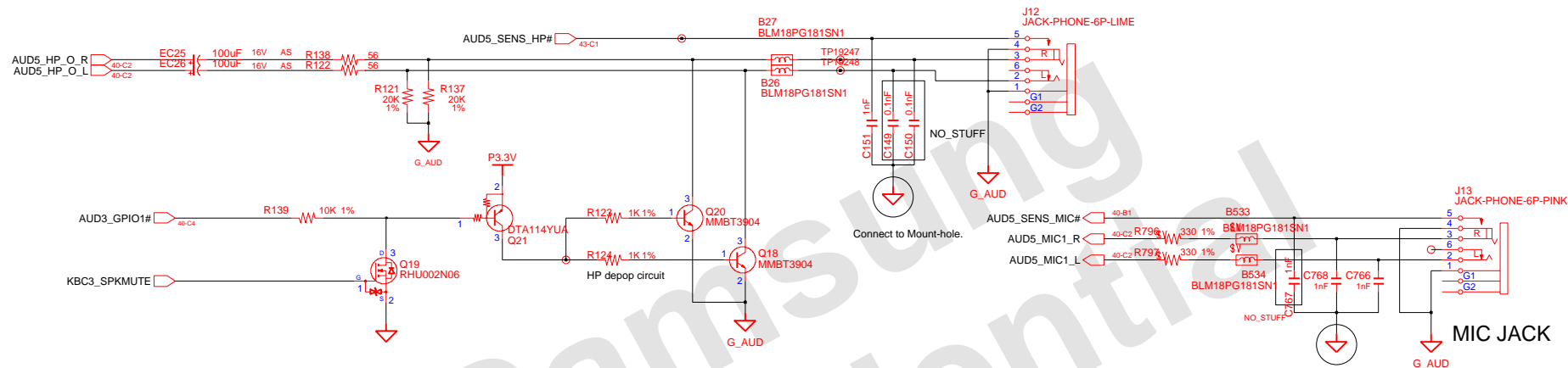
INTERNAL STEREO SPEAKERS



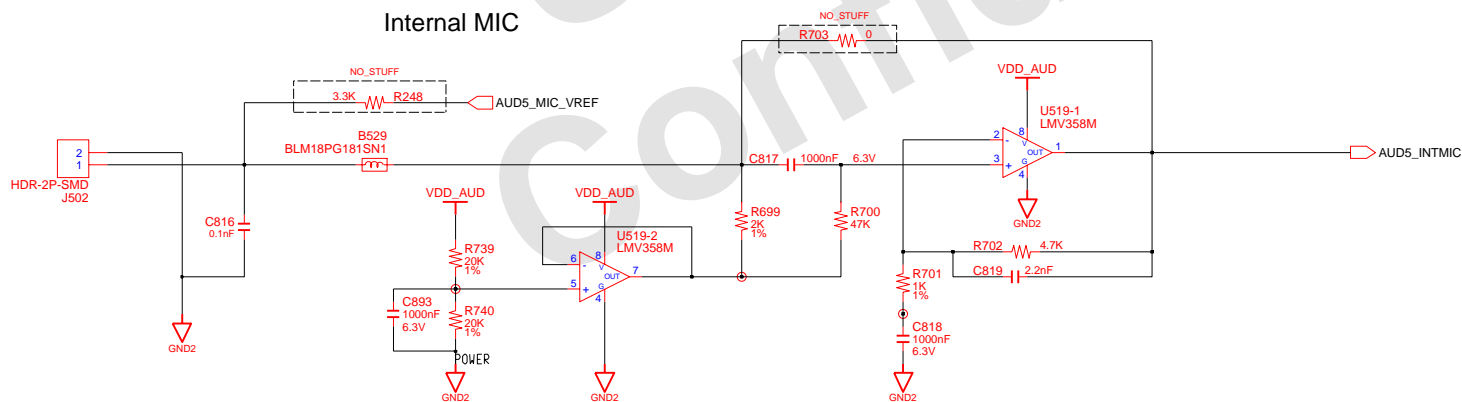
DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena AUDIO AMP	SAMSUNG ELECTRONICS
CHECK	WUSHUIJANG	DEV. STEP	PV2			PART NO. BA41-XXXXX
APPROVAL	KEVIN LEE	REV	1.0			
MODULE CODE		LAST EDIT	October 23, 2007 10:38:02 AM	PAGE	39	OF 58

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HEADPHONE



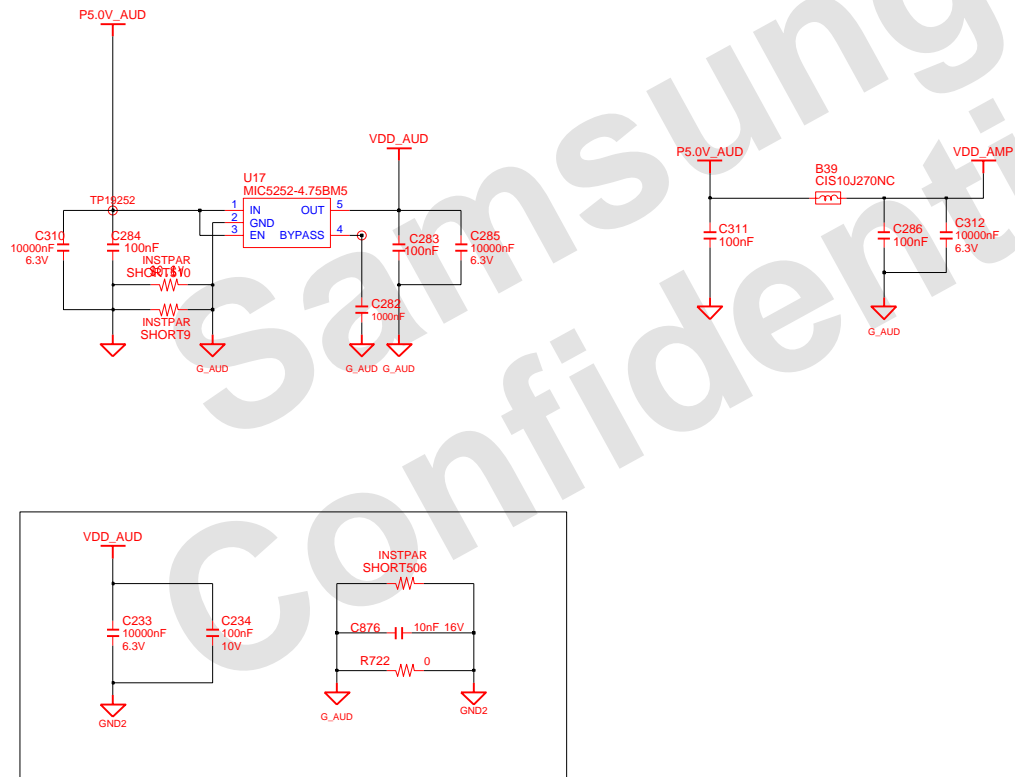
Internal MIC



DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena	SAMSUNG ELECTRONICS
CHECK	WUSHUJIANG	DEV. STEP	PV2		HEAD PHONE JACK	
APPROVAL	KEVIN LEE	REV	1.0		AND MIC JACK	
MODULE CODE		LAST EDIT				
October 23, 2007 10:38:02 AM						PAGE 40 OF 58

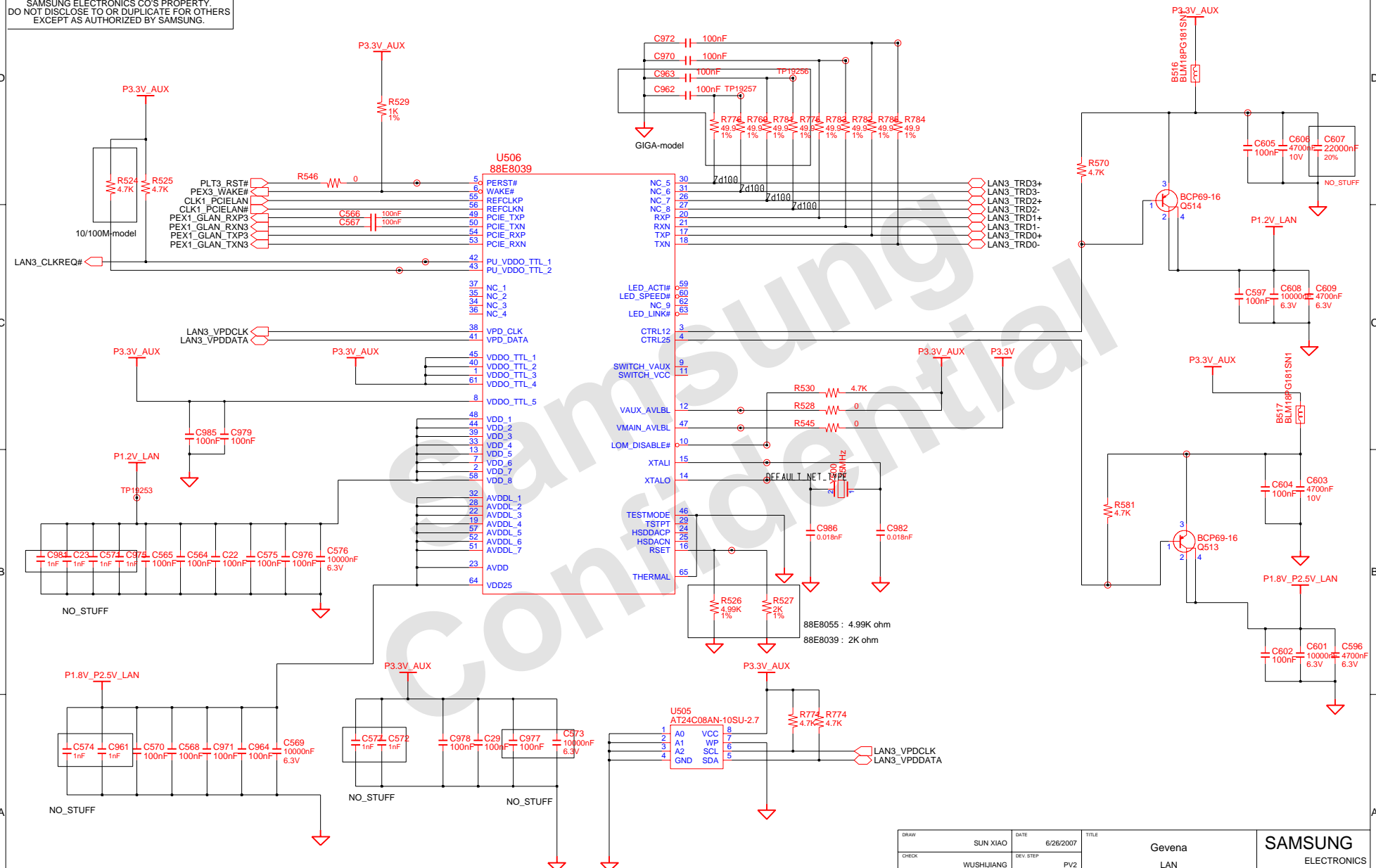
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AUDIO POWER



DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena AUDIO AUDIO POWER	SAMSUNG ELECTRONICS
CHECK	WUSHUJIANG	DEV. STEP	PV2			PART NO. BA41-XXXXX
APPROVAL	KEVIN LEE	REV	1.0			
MODULE CODE		LAST EDIT	October 23, 2007 10:38:02 AM	PAGE	41	OF 58

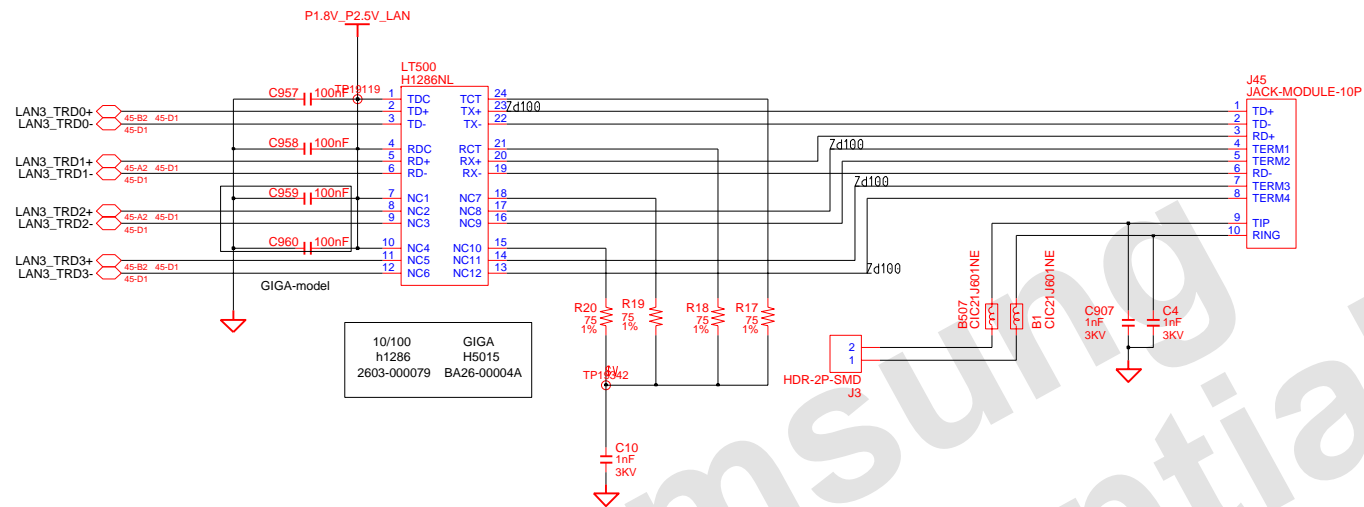
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DRAW	SUN XIAO	DATE	6/26/2007	<div>Gevena LAN 88E8055</div> <div>SAMSUNG ELECTRONICS</div>			
CHECK	WUSHUJIANG	DEV STEP	PV2				
APPROVAL	KEVIN LEE	REV	1.0			<div>PART NO.</div> <div>BA41-XXXXX</div>	
MODULE CODE		LAST EDIT		October 23, 2007 10:38:02 AM	PAGE	42	OF 58

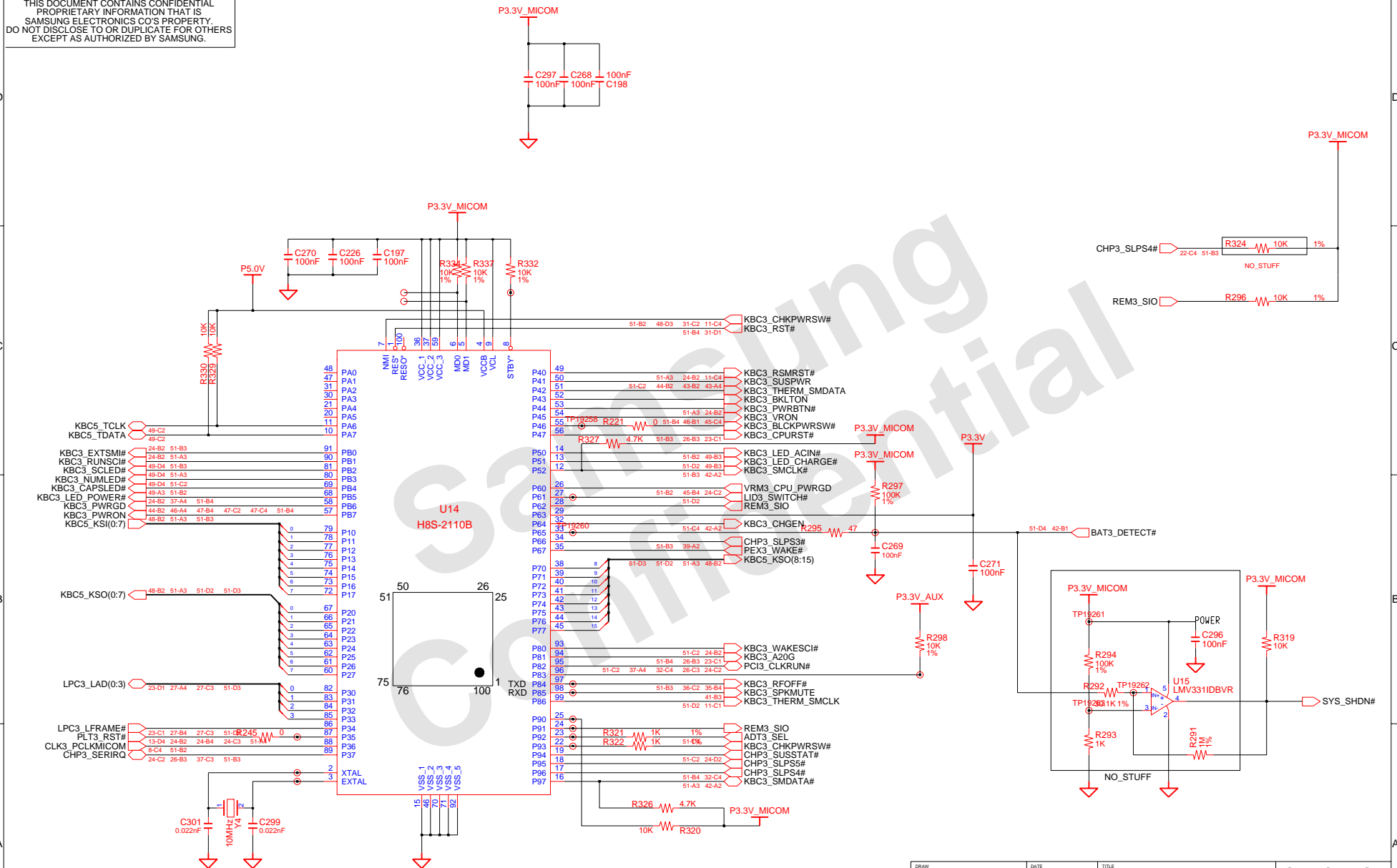
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The distance between LAN controller
and transformer is designed to extend less than two inches.



DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena LAN	SAMSUNG ELECTRONICS
CHECK	WUSHUIJANG	DEV. STEP	PV2			
APPROVAL	KEVIN LEE	REV	1.0		LAN JACK RJ45	PART NO. BA41-XXXXX
MODULE CODE		LAST EDIT	October 23, 2007 10:38:02 AM	PAGE	43	OF 58

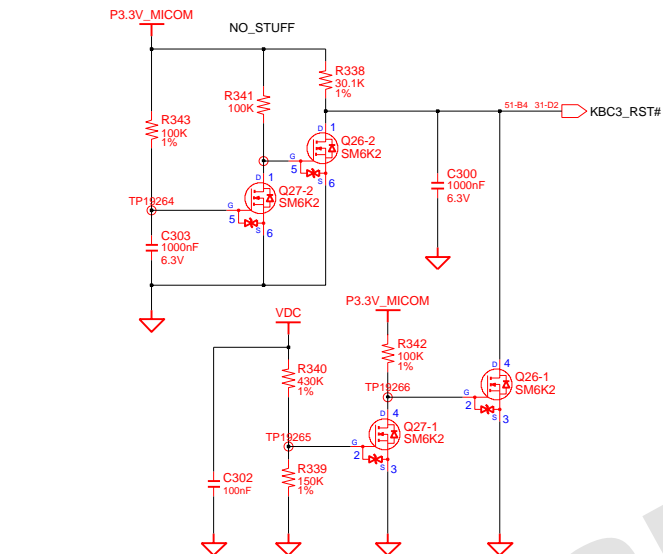
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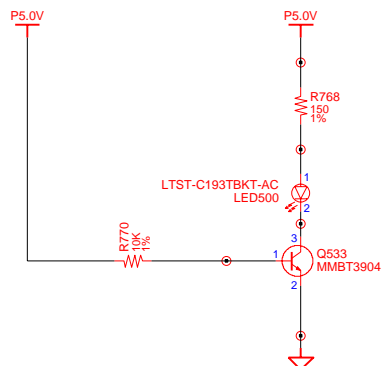
DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena	SAMSUNG
CHECK	WUSHUJIANG	DEV. STEP	PV2		MICOM	ELECTRONICS
APPROVAL	KEVIN LEE	REV	1.0		211B	PART NO.
MODULE CODE		LAST EDIT				BA41-XXXXX
				October 23, 2007 10:38:02 AM	PAGE	44 OF 58

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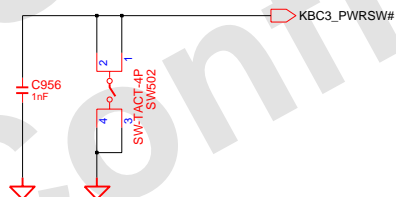
MICOM RESET



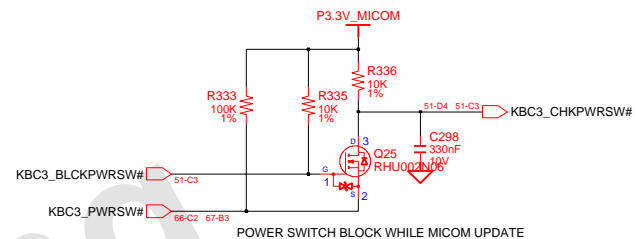
POWER ON LED



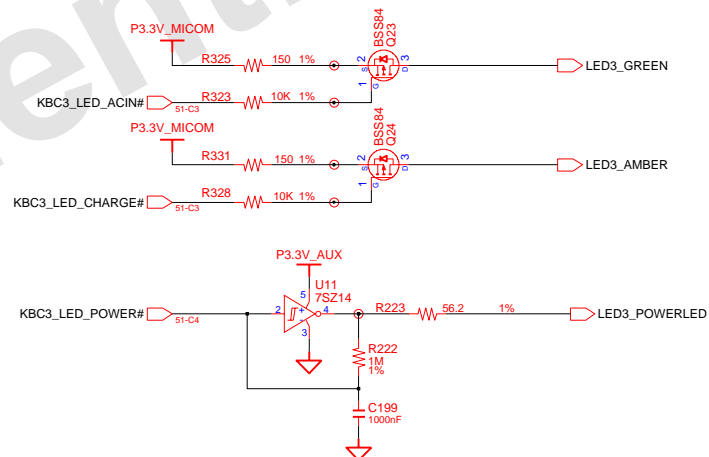
POWER ON SW BUTTON



FOR MICOM UPDATE

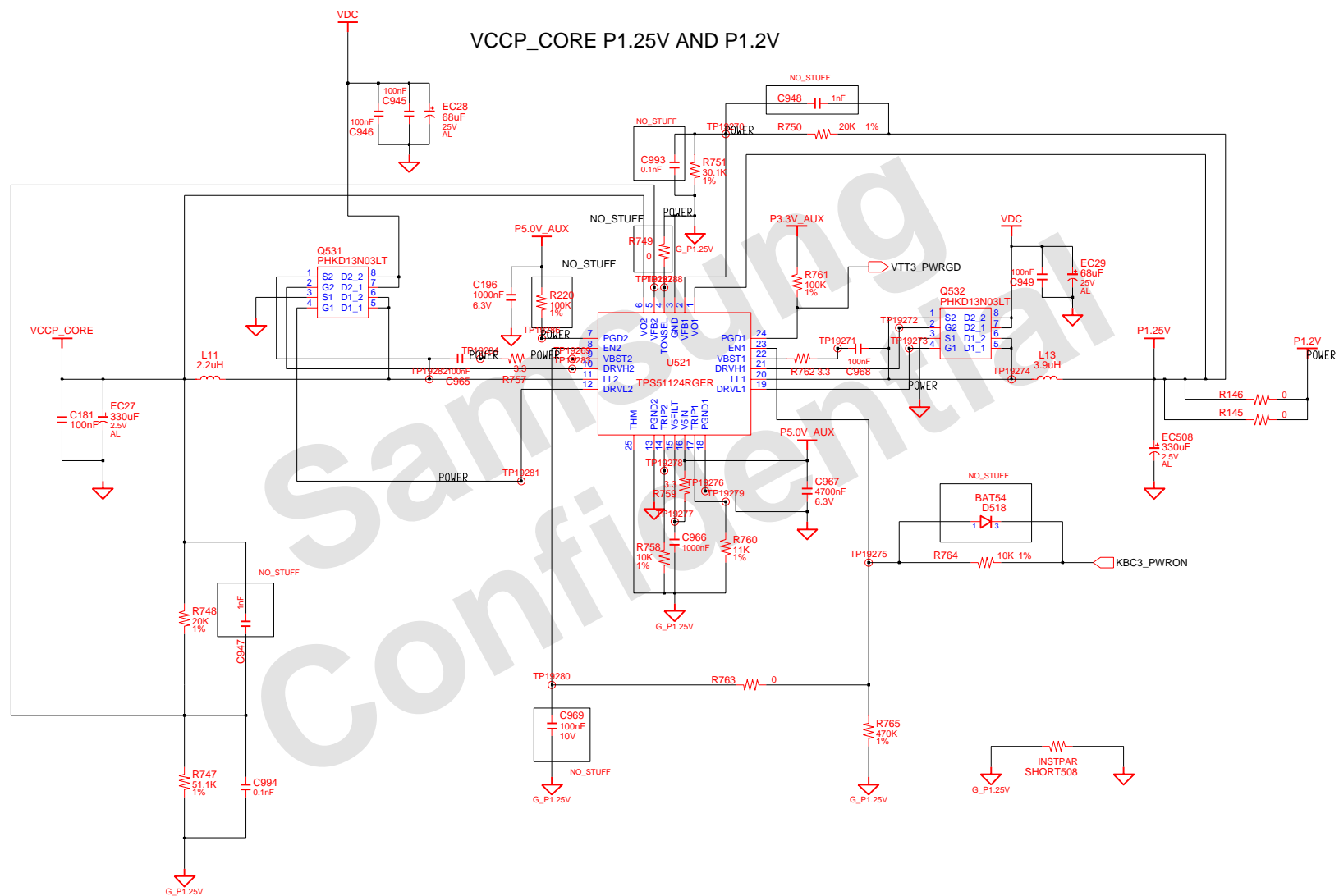


ADAPTERIN/CHARGING LED



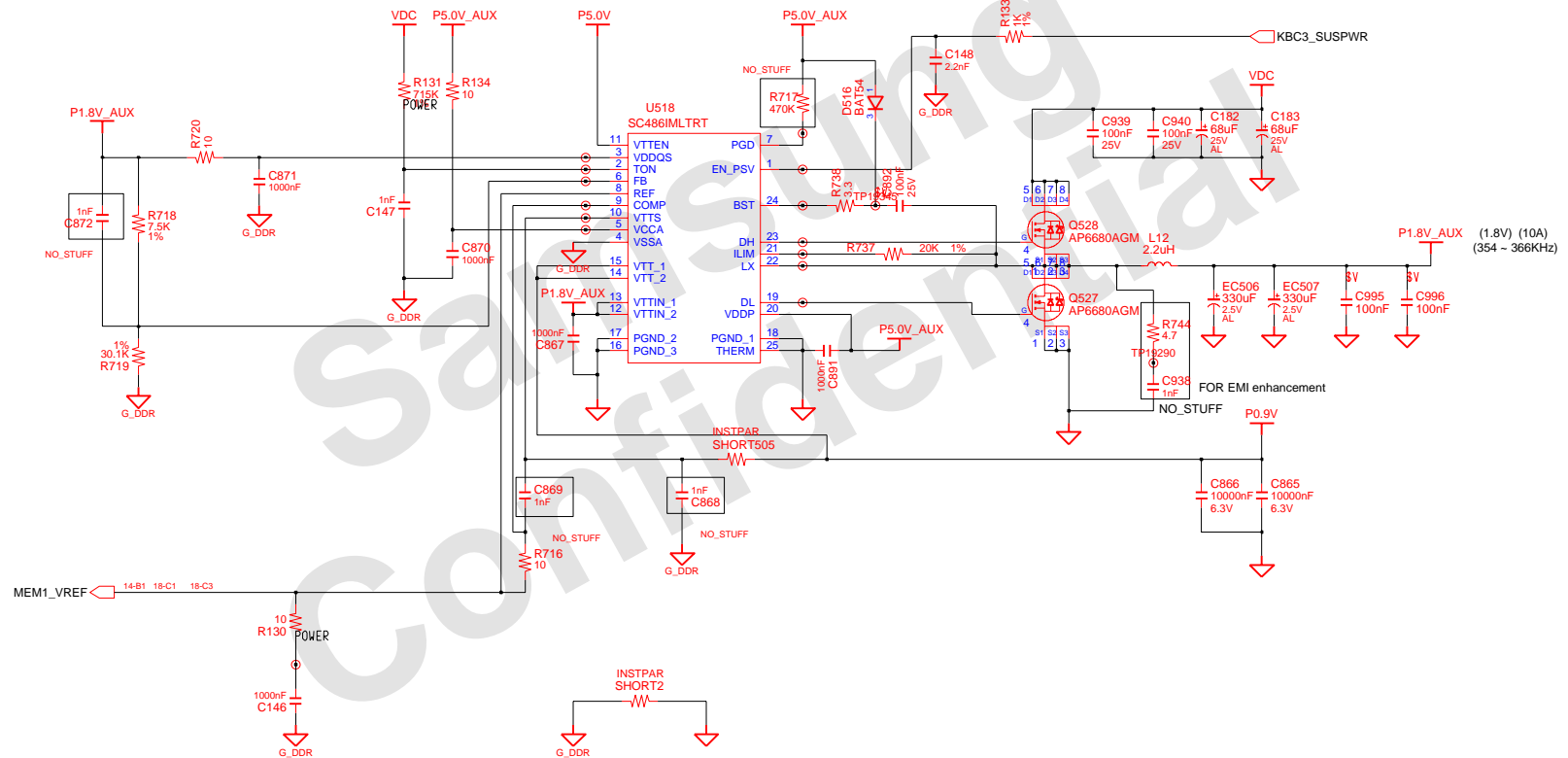
DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena	SAMSUNG ELECTRONICS
CHECK	WUSHUJIANG	DEV. STEP	PV2		MICOM	
APPROVAL	KEVIN LEE	REV	1.0		MICOM LOGIC SCH	
MODULE CODE		LAST EDIT				
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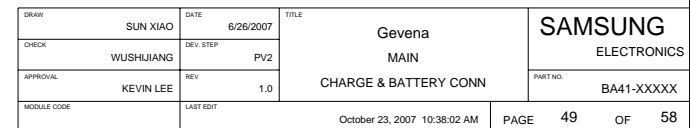
DRAWN	SUN XIAO	DATE	6/26/2007	Gevena MAIN VCCP P1.25V AND P1.2V		SAMSUNG ELECTRONICS			
CHECK	WUSHUJIANG	DEV. STEP	PV2					PART NO.	BA41-XXXXX
APPROVAL	KEVIN LEE	REV	1.0			October 23, 2007 10:38:02 AM		PAGE	47
MODULE CODE		LAST EDIT							

DDR2 Power



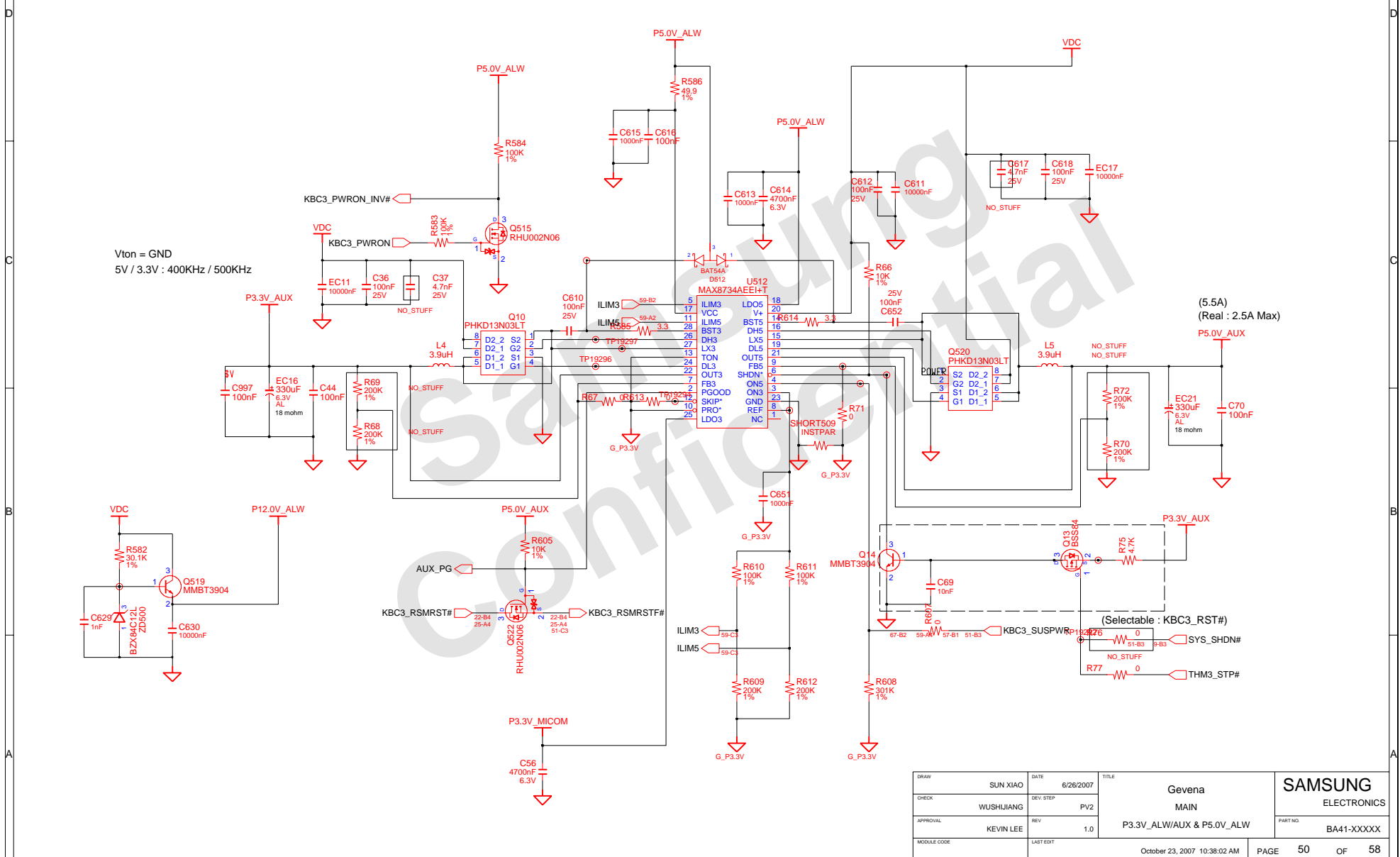
DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena MAIN	SAMSUNG ELECTRONICS
CHECK	WUSHUIJANG	DEV. STEP	PV2			PART NO. BA41-XXXXX
APPROVAL	KEVIN LEE	REV	1.0		DDR2 POWER	
MODULE CODE		LAST EDIT				
				October 23, 2007 10:38:02 AM	PAGE 48 OF 58	

CHARGER & POWER MANAGEMENT



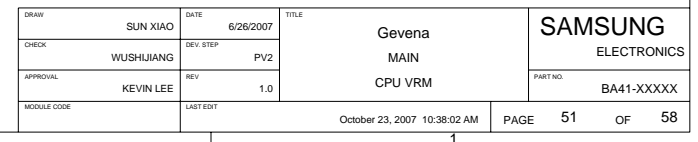
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P3.3V_ALW/AUX & P5V_AUX



DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena	SAMSUNG
CHECK	WUSHUJIANG	DEV. STEP	PV2	MAIN	MAIN	ELECTRONICS
APPROVAL	KEVIN LEE	REV	1.0	P3.3V_ALW/AUX & P5.0V_ALW	PART NO.	BA41-XXXXX
MODULE CODE		LAST EDIT		October 23, 2007 10:38:02 AM	PAGE	50 OF 58

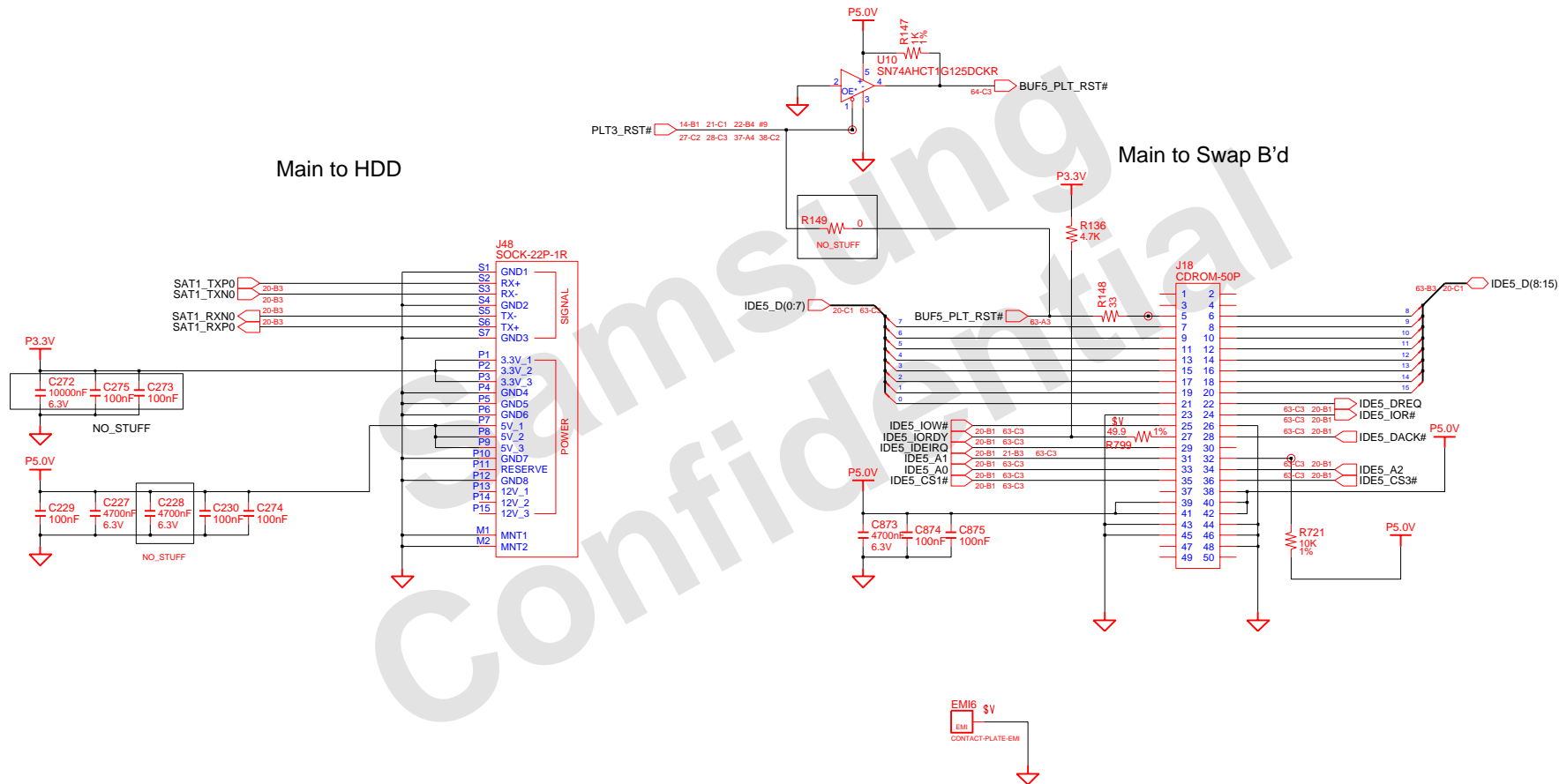
CPU VRM [SEMTECH]



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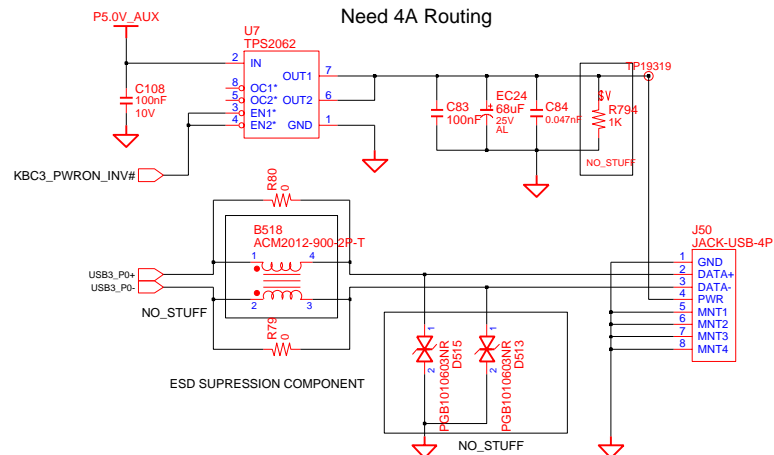
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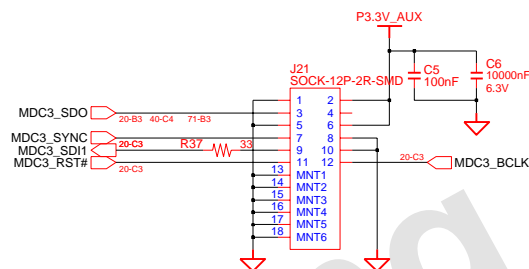
DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena	SAMSUNG ELECTRONICS
CHECK	WUSHUJIANG	DEV. STEP	PV2	CONNECTOR	CONNECTION	
APPROVAL	KEVIN LEE	REV	1.0	HDD & ODD CONNECTOR	PART NO.	BA41-XXXXX
MODULE CODE		LAST EDIT	October 23, 2007 10:38:02 AM	PAGE	53	OF 58

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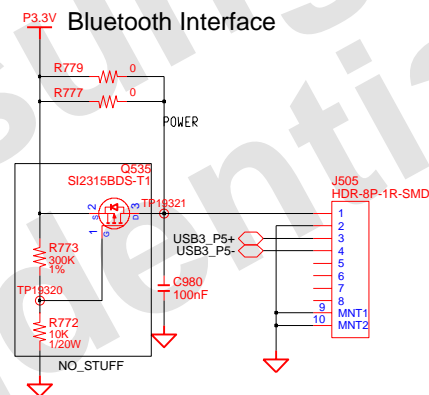
1 PORT USB CONNECTOR



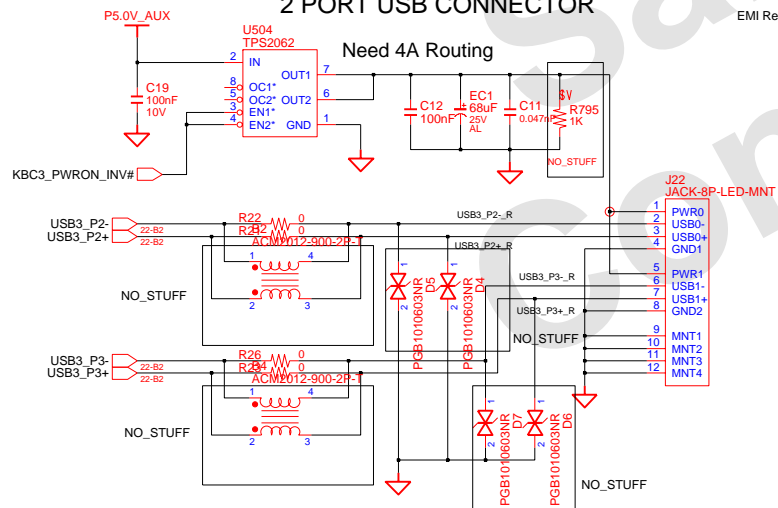
MDC Connector



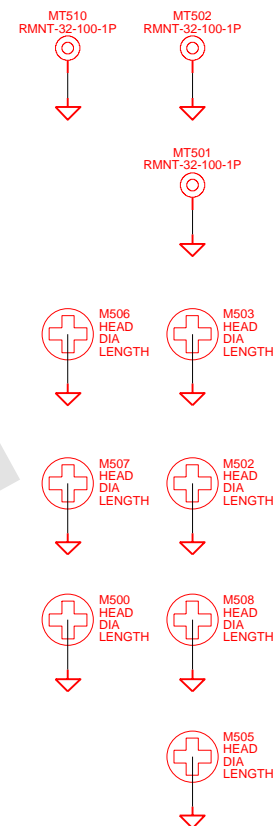
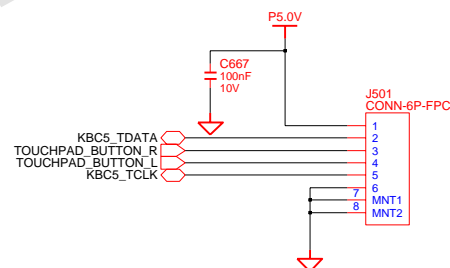
Bluetooth Interface



2 PORT USB CONNECTOR

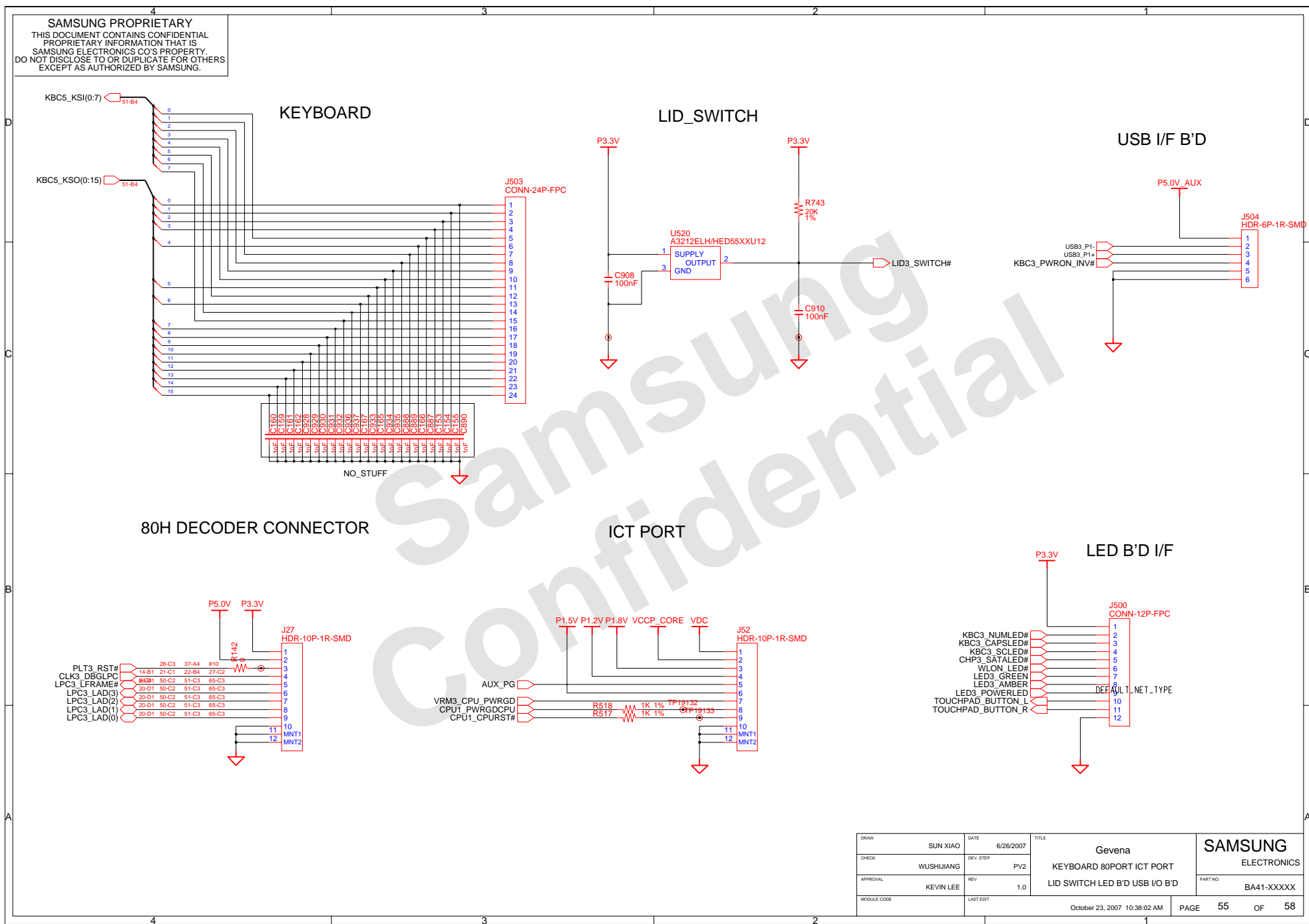


TOUCHPAD CONNECTOR



DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena	SAMSUNG
CHECK	WUSHUJIANG	DEV. STEP	PV2	USB MDC &	USB MDC &	ELECTRONICS
APPROVAL	KEVIN LEE	REV	1.0	TOUCHPAD BLUETOOTH I/F	PART NO.	BA41-XXXXX
MODULE CODE		LAST EDIT		October 23, 2007 10:38:02 AM	PAGE	54 OF 58

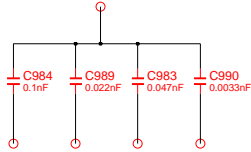
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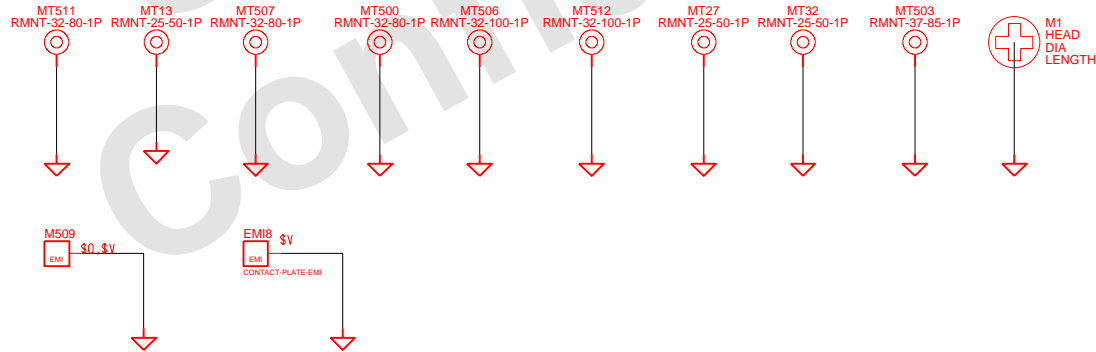
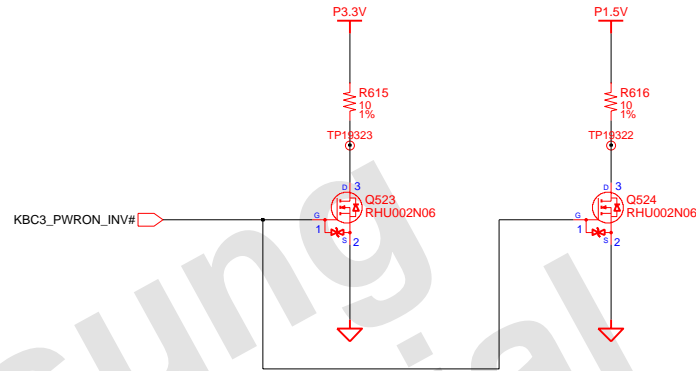
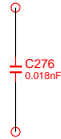
DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena	SAMSUNG
CHECK	WUSHUJIANG	DEV. STEP	PV2	KEYBOARD 80PORT ICT PORT		ELECTRONICS
APPROVAL	KEVIN LEE	REV	1.0	LID SWITCH LED B'D USB I/O B'D	PART NO.	BA41-XXXXX
MODULE CODE		LAST EDIT	October 23, 2007 10:38:02 AM	PAGE	55	OF 58

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TOP SIDE



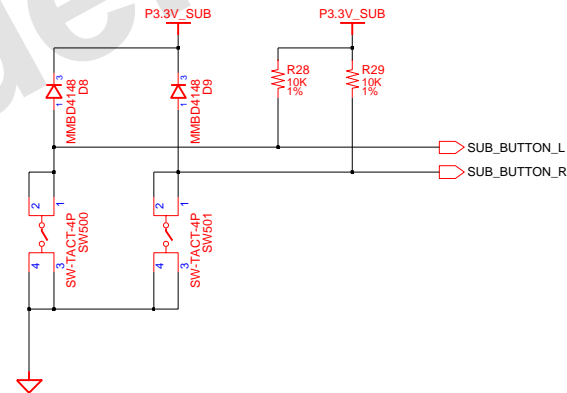
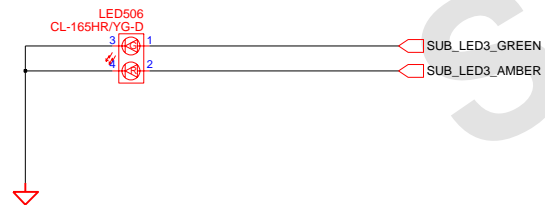
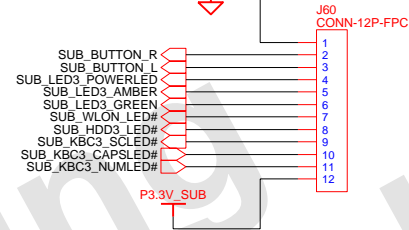
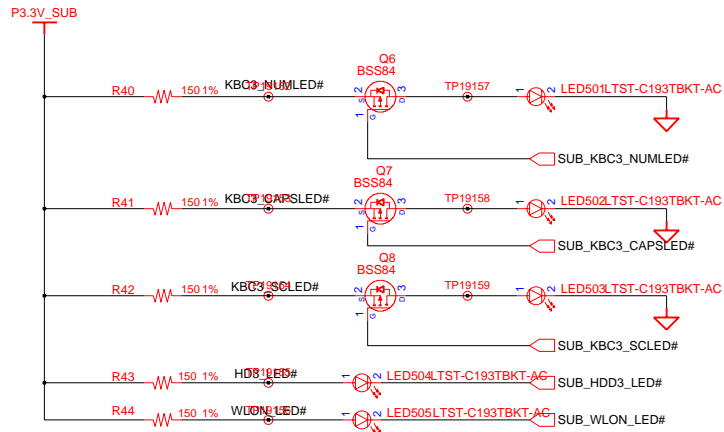
BOTTOM SIDE



DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Gevena OTHERS	SAMSUNG ELECTRONICS PART NO. BA41-XXXXX
CHECK	WUSHIJIANG	DEV. STEP	PV2			
APPROVAL	KEVIN LEE	REV	1.0			
MODULE CODE		LAST EDIT	October 23, 2007 10:38:02 AM	PAGE	56 OF 58	

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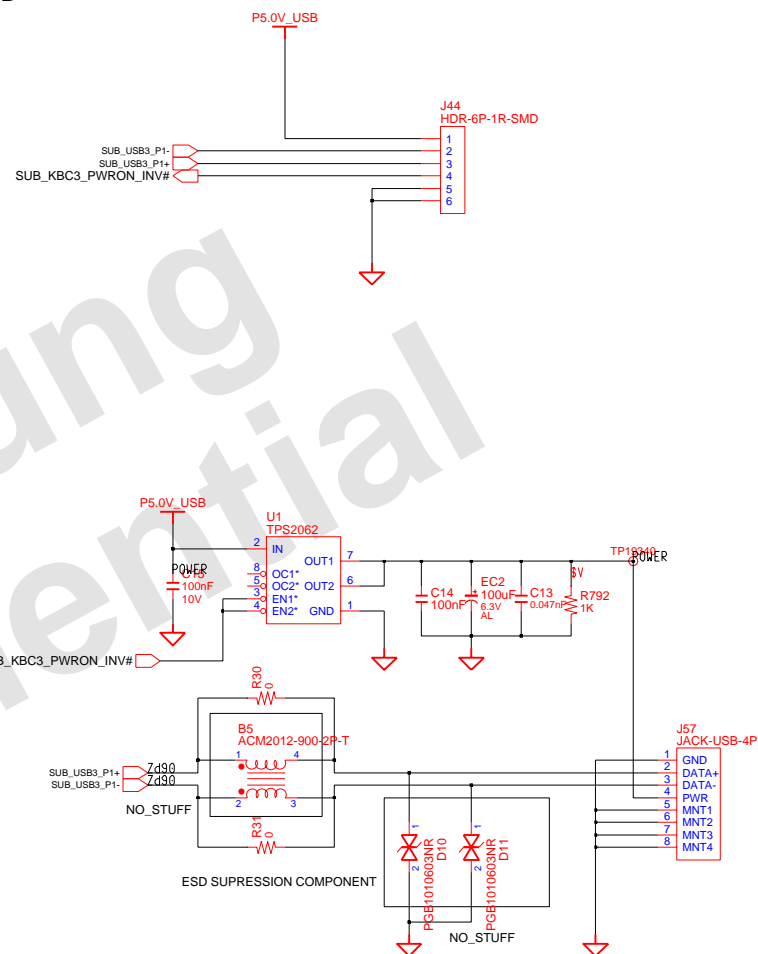
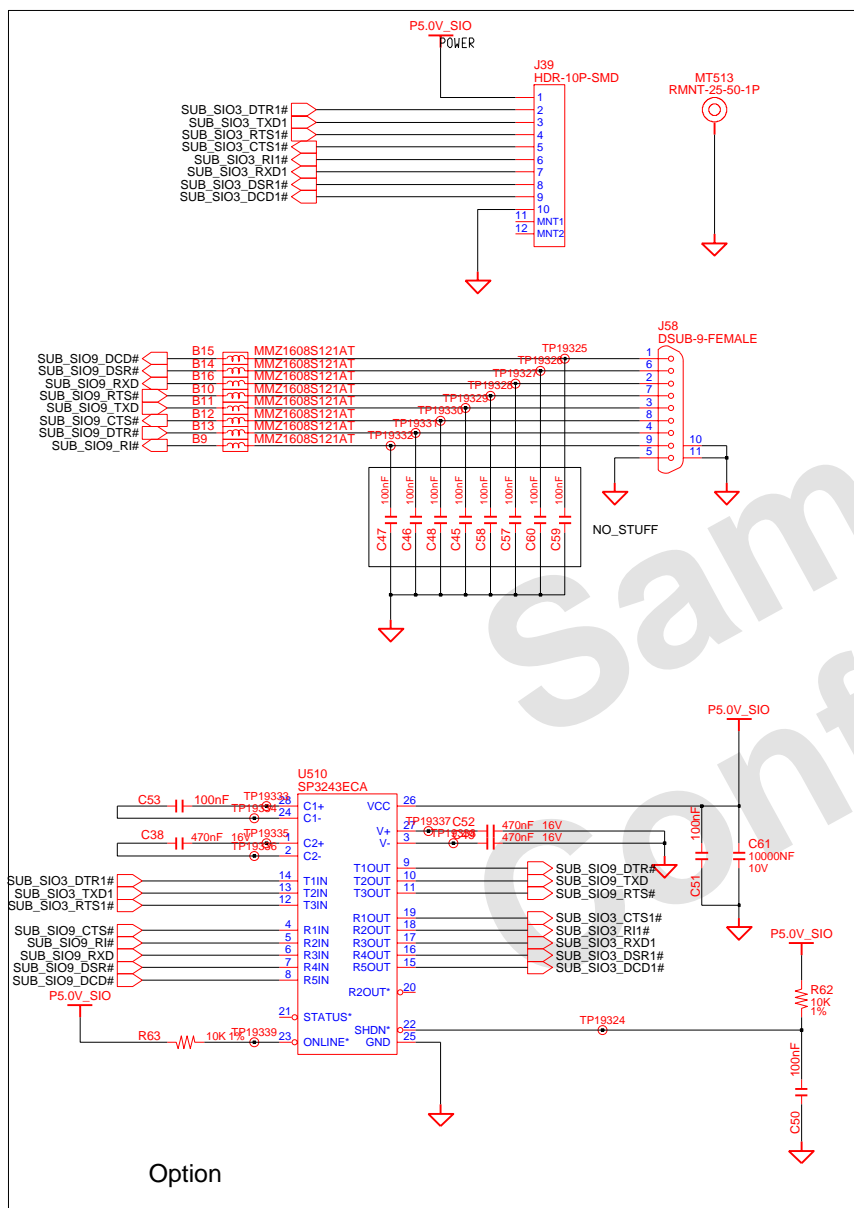
TOUCHPAD AND LED B'D



DRAW	SUN XIAO	DATE	6/26/2007	TITLE	Geneva	SAMSUNG ELECTRONICS PART NO. BA41-
CHECK	WUSHIJIANG	DEV. STEP	PV2	TOUCHPAD AND LED B'D		
APPROVAL	KEVIN LEE	REV	1.0			
MODULE CODE	LAST EDIT		October 23, 2007 10:38:02 AM	PAGE	57 OF 60	

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SIO AND USB SUB B'D



DRAW	SUN XIAO	DATE	6/30/2007	TITLE Geneva MIO BOARD USB AND SIO SUB B'D	SAMSUNG ELECTRONICS
CHECK	WUSHIJIANG	DEV. STEP	PV2		
APPROVAL	KEVIN LEE	REV	1.0		
MODULE CODE	LAST EDIT		October 23, 2007 10:38:02 AM		
				PAGE	58 OF 60

TP18380OAU3_SEL
TP18381OAU3_BCLK
TP18382OAU3_BEEP
TP18383OAU3_BEEP_CU
TP18384OAU3_GP100#
TP18385OAU3_GP101#
TP18386OAU3_GP101#_L
TP18387OAU3_RST#
TP18388OAU3_SDIO
TP18389OAU3_SDIO_RU
TP18390OAU3_SDO
TP18391OAU3_SPKR

TP18393OAU3_SYNC
TP18394OAU5_HP_O_L
TP18395OAU5_HP_O_L_CR
TP18396OAU5_HP_O_L_RB
TP18397OAU5_HP_O_B
TP18398OAU5_HP_O_B_CR
TP18399OAU5_HP_O_B_RB
TP18400OAU5_INTMIC
TP18401OAU5_L_LINE_O_L
TP18402OAU5_L_LINE_O_L_CU
TP18403OAU5_L_LINE_O_L_C
TP18404OAU5_L_O_L_CU
TP18405OAU5_MIC1_L
TP18406OAU5_MIC1_L_BCON
TP18407OAU5_MIC1_L_CU
TP18408OAU5_MIC1_R
TP18409OAU5_MIC1_R_BCON
TP18410OAU5_MIC1_R_CU
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TP18362OBA13_SMDATA#
TP18363OBA13_CONN_TP_BB
TP18364OBU5_PLT_RST#

TP18367OCHP1_5_DMICOMP_R
TP18368OCHP3_BIOSWP#
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TP18379OCHP3_GP1012
TP18328OCHP3_GP1017
TP18329OCHP3_INTRUDER#
TP18330OCHP3_INTVEMEN
TP18331OCHP3_LANT100_SLP
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TP18333OCHP3_LDR01#
TP18334OCHP3_PC1STP#
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TP18336OCHP3_R1CRST#
TP18337OCHP3_SATACLKREQ#
TP18338OCHP3_SATALED#
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TP18340OCHP3_SLP3#
TP18341OCHP3_SLP5#
TP18342OCHP3_SLP5#
TP18343OCHP3_SUSSTAT#

TP18344OCHP3_TPT_R
TP18345OCHP3_USBRRIAS_R
TP18346OCHP3_USBRROC9#_R
TP18347OCHP3_SDATAOUT0_R
TP18319OCLK3_DBLPC
TP18320OCLK3_TCH14
TP18321OCLK3_PCLKICH
TP18322OCLK3_PCLKMICOM
TP18323OCLK3_PCLKSIO
TP18324OCLK3_PCLKSIO_DS
TP18325OCLK3_PWRCD
TP18326OCLK3_S1014
TP18327OCLK3_USB48
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TP18309OCPU1_BSEL2
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TP18311OCPU1_COMP1_R
TP18312OCPU1_COMP2_R
TP18313OCPU1_COMP3_R
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TP18251OCPU2_THERMDC
TP18252OCPU3_THRMTRIP#
TP18253OCPU_CORE_HG2
TP18254OCPU_CORE_LG1
TP18255OCPU_CORE_LG2
TP18256OCPU_CORE_PHASE_2

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TP17771ODE5_IOW#
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TP17833OKBC5_TLAD(99)

DRAW	SUNXIAO	DATE	9/10/2007	TITLE	Gevena TEST POINT	SAMSUNG ELECTRONICS PART NO. BA41 - undef ined
CHECK	WUSHIJIANG	DEV. STEP	PV2			
APPROVAL	KEVIN.LEE	REV	1.0			
MODULE CODE		LAST EDIT	October 23, 2007 10:38:02 AM	PAGE	59 OF 59	

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TP1#8605#MCH1.HRCOMP#
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TP1#8609#MCH1.HXSING
TP1#8610#MCH1.VITL1F_C
TP1#8611#MCH1.VITL2F_C
TP1#8585#MCH1.VITL1F_3_C
TP1#8586#MCH3.BMBSU#
TP1#8587#MCH3.CLKREQ#
TP1#8588#MCH3.CL_VREF
TP1#8589#MCH3.EXITSS#
TP1#8590#MCH3.EXITSS#
TP1#8591#MCH3.ICHSYNCH#
TP1#8592#MCH3.ICHSYNCH#_R
TP1#8593#MCH1.TEST1_R
TP1#8594#MCH1.TEST2_R
TP1#8595#MDC3.BCLK
TP1#8596#MDC3.RS#
TP1#8597#MDC3.SD11
TP1#8598#MDC3.SD11_R
TP1#8599#MDC3.SD0
TP1#8600#MDC3.SYNC
TP1#8591#SAI_R
TP1#8538#MCH1.VREF
TP1#8539#MIN3.CLKREQ#

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TP18541 ○ MODEM_TIP_BCON

[illegible]

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T#186193 PC1_5V_CRT_TYD  
T#186194 PC1_5V_GLAN_CMPIO_R  
T#186195 PC1_8V_AUX_RCOPM#_R  
T#186196 PC1_8V_AUX_RCOPM_E  
T#186197 PC1_8V_AUX_RCOPM_VOH_R  
T#186198 PC1_8V_AUX_RCOPM_VOL_R  
T#186199 PC1_8V_AUX_VCC_SM_CK  
T#186200 PS_0V_ALW_SREF_SUS  
T#186201 PS_0V_ALW_BS1  
T#186202 PS_0V_AUX_HG  
T#186203 PS_0V_AUX_LG  
T#186204 PS_0V_AUX_PHASE  
T#186205 PS_0V_AUX_PSR  
T#186206 PS_0V_CLKRUN#  
T#186207 PC13_DEVSEL#  
T#186208 PC13_FRAME#  
T#186209 PC13_CNTIO#  
T#186210 PC13_INTH#  
T#186211 PC13_INTB#  
T#186212 PC13_INTC#  
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T#186214 PC13_INTE#  
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T#186216 PC13_INTG#  
T#186217 PC13_INTH#  
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T#186220 PC13_IRQD#  
T#186221 PC13_IRQE#  
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T#186223 PC13_IRQG#  
T#186224 PC13_IRQH#  
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T#186226 PC13_IRQJ#  
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TP18053 OPEX3_WAKE#
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TP180570 SC452 CS1-
 TP180121 SC452 HYS
 TP180222 SC452 BS11
 TP180223 SC452 BS12
 TP180224 SC452 BS13 RC
 TP180225 SC452 BS14
 TP180226 SC452 CS2-
 TP180227 SC452 DA2
 TP180228 SC452 GSP
 TP180302 SC452 DPST PW
 TP180302 SC452 DRP+
 TP180313 SC452 DRP-
 TP180322 SC452 ERKQUT
 TP180323 SC452 ERKQUT
 TP180342 SC452 FB-
 TP180352 SC452 ISH
 TP180362 SC452 SS-
 TP180363 SC452 SS-
 TP180364 SC452 V1
 TP180365 SC452 VP2N2
 TP180392 SC452 VREF
 TP180402 SC103 CDS1
 TP180412 SC103 CDS1
 TP180413 SC103 CDS1
 TP180432 SC103 DIR1
 TP180442 SC103 RT1
 TP180452 SC103 RT1
 TP180453 SC103 RT1
 TP180472 SC103 TXD1
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TP19054VRVR33_CPU_PWRGD
TP19055VTVT13_PWRGD
TP18230MLNLED_#
TP18232IO_T0_VDDIOA
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TP18241CND2
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TP18245OC_AUD
TP18198OC_CPU
TP18200OC_CPU
TP18204OC_DDR
TP18206OC_CPU
TP18212OC_P1_5V
TP18217OC_P3_3V
TP18222LCD_VDD03V
TP18223LCD_VDD03V
TP18224OC_P2_5V
TP18225OC_P2_5V
TP18116PRTC_BAT
TP18122OV_PSS_PL1_VDD
TP18124OVCCP_CORE
TP18125OVCCP_CORE
TP18130OVCC_CRT
TP18131OVCC_CRT
TP18081OVDC
TP18084OVDC_ADPT
TP18085OVDC_INV
TP18086OVDC_INV
TP18098OVDD_AUD

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TP18164OP0.9V
TP18170OP1.05V_PEG
TP18172OP1.25V
TP18178OP1.2V
TP18183OP1.5V
TP18187OP1.5V_EXP
TP18188OP1.8V
TP18192OP1.8V_ALW
TP18134OP12.0V_ALW
TP18136OP3.3V_ALW
TP18141OP3.3V_AUX_EXP
TP18146OP3.3V_EXP
TP18150OP3.3V_MCD
TP18152OP3.3V_MICOM
TP18158OP3.3V_USB
TP18161OP5.0V_ALW
TP18104OP5.0V_ALW
TP18109OP5.0V_SIO
TP18112OP5.0V_USB

DRAW	SUNXIAO,	DATE	9/10/2007	TITLE	Gevena TEST POINT	SAMSUNG ELECTRONICS	PART NO.	BA41-undef i
CHECK	WUSHIJIANG,	DEV. STEP	PV2					
APPROVAL	KEVIN.LEE,	REV	1.0					
MODULE CODE	LAST EDIT							

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